Satellite/Terrestrial Digital Demodulation and Correction IC

TC90512XBG

Application Note

(rev.103)

This application note contains important information about using the TC90512, together with practical examples.
Please refer to the latest application note for the product.

Contents

*** Blue text indicates changes from the TC90502XBG or changes in past versions.**

*** Red text indicates corrections for the current version.**

1. Overview

This manual describes simple application examples for the TC90512XBG terrestrial digital and BS digital demodulation and correction IC (abbreviated below as the TC90512).

2. Satellite Digital Reception

2.1 Initialization

The satellite digital (PSK) demodulation function of the TC90512 is turned on in the initial state.

If halting BS reception to reduce power consumption, please use the PSK demodulation standby function. The standby function is described in section 8.2 of the specification. Three different modes are available in standby. These are continuous sleep mode, intermittent operation mode, and intermittent operation + monitoring for activation in the event of an emergency warning broadcast signal. If jspladc = "1" is set, the AD converter circuit also powers down during the sleep state to further reduce power consumption.

Setting psksyrst = "1" initializes all of the registers in the PSK demodulator unit. (Setting psksyrst = "1" is required in addition to the SYRSTN power-on reset when the power is turned on.) Do not set the registers until 1μs or more has elapsed after the above power-on reset completes. Similarly, set psksyrst = "1" first, before setting any other PSK registers.

[Important] Always set psksyrst = "1" before setting any other registers in the PSK unit.

For BS reception, using TMCC for external control is not required other than for getting and selecting (specifying) the TS_ID. The level information and other parameters transferred by TMCC are obtained automatically in the TC90512 and used to control the demodulation circuit. If no TS_ID is specified, or if the specified TS_ID does not exist, the TS data in the first slot of the transmitted frame is output automatically.

The TC90512 optimizes control by selecting the carrier regeneration loop gain automatically for 8PSK, QPSK, and BPSK modulation. Set the loop gains for QPSK and BPSK modulation in the pllqhgd and pllbhgd registers respectively. Also set the upper limit for the loop gain control in the pllhmax register.

Always set the following values beforehand.

Set 1Bh in the pllbhgd register

Address 52h	Initial value 8Ah	Setting value 89h
Address 53h	Initial value 13h	Setting value B3h

Set 1Dh in the pllqhgd register

Address 5Ah	Initial value 2Eh	Setting value 2Dh
Address 5Bh	Initial value 23h	Setting value D3h

Set Bh in the pllhmax register

Address 51h	Initial value C0h	Setting value B0h

[Important] Always set 89h, B3h, 2Dh, and D3h in PSK addresses 51h, 52h, 53h, 5Ah, and 5Bh respectively.

2.2 Channel Selection

Figure 2-1 shows an example of the basic channel selection flowchart for BS demodulation mode.

Set a PSK demodulation reset (pskmsrst="1") when performing BS channel selection. As the reset is set back to "0" automatically after 4μs, you do not need to set "0" to end the reset. Similarly, no wait time is required for I^2C communications after the reset.

Although the main demodulation operation is performed without any external software control after a demodulation reset, use a timer in the external microcomputer to determine whether reception is not available (**reception is not available for one second after a demodulation reset**). If you want to confirm that TS output is error free, this can be performed using rlockh (for upper level) and rlockl (for lower level)

Figure 2-2 shows an example in which control flow has been added to use the tuner to adjust for the frequency deviation in the frequency down-converter. Please take account of the tuner's filter bandwidth and its step frequency for channel selection when setting the tolerance for frequency deviation.

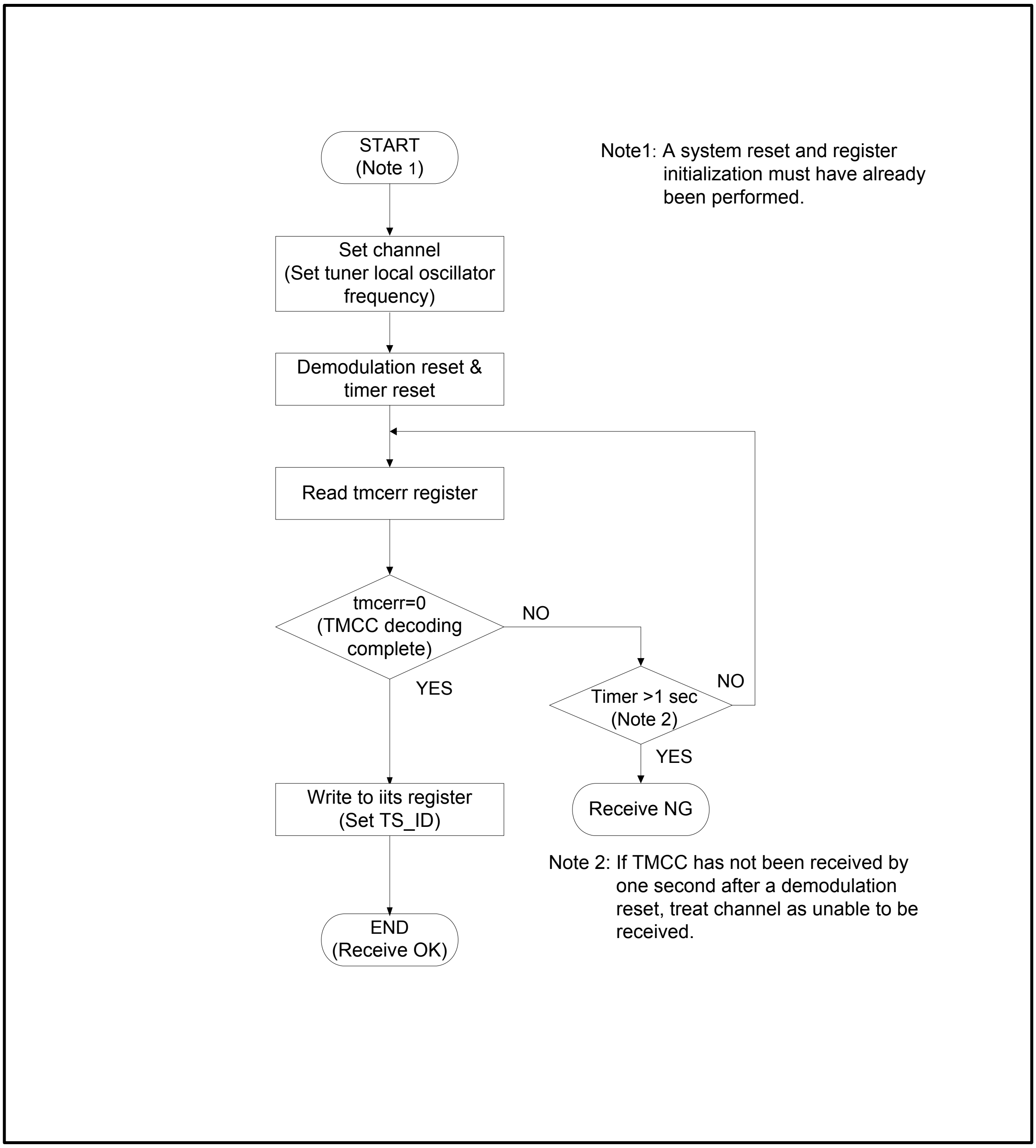
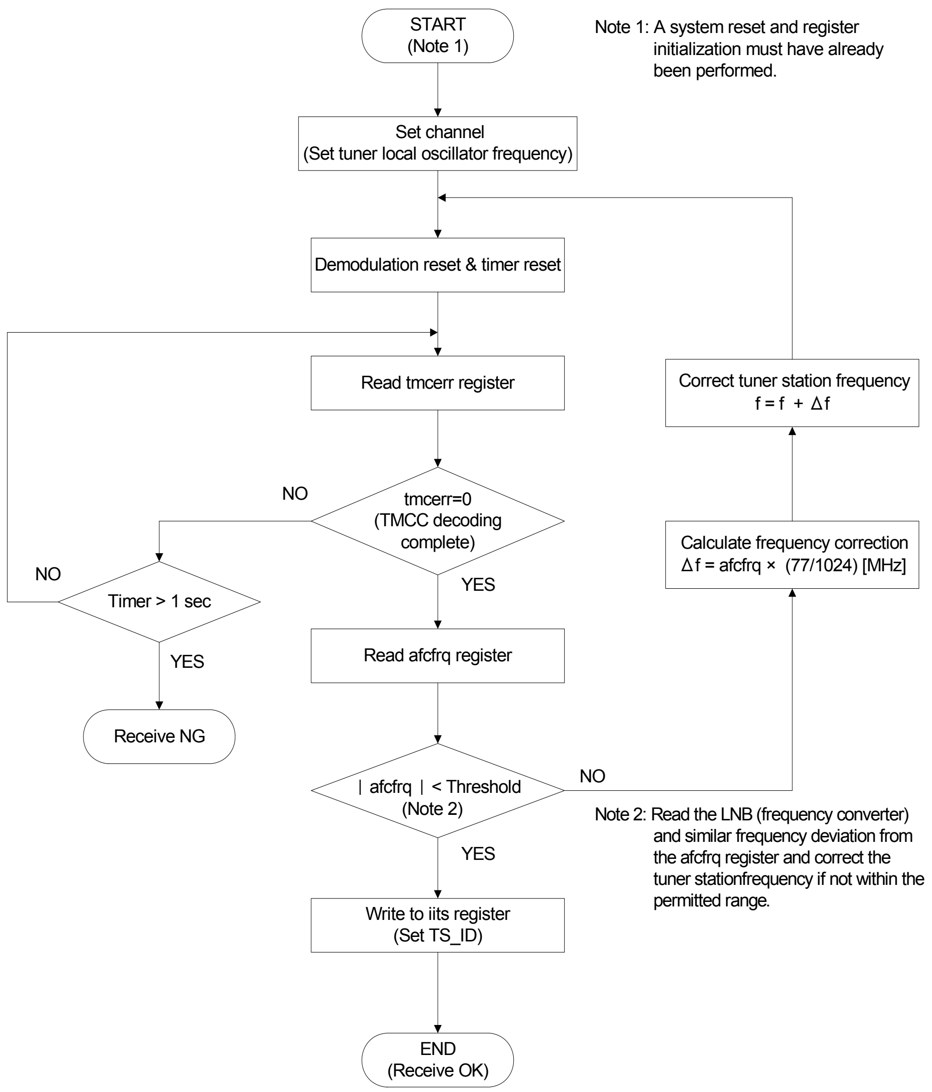


Figure 2-1 Basic Channel Selection Flowchart for BS Demodulation



Figur

e 2-2 Channel Selection Flowchart for BS Demodulation Including Correction of Frequency Deviation

2.3 AGC Control

Some of the AGC control register settings need to be modified to match the tuner you are using. Example settings are described below.

2.3.1 AGC Limiter Setting

The AGC limiter function is used when the characteristics of the AGC amplifier are such that saturation can occur. The function can be used to prevent a sudden reduction in AGC control sensitivity and deterioration of control response in the region where saturation occurs. Use the aglmax and aglmin registers to set the upper and lower limits respectively for the AGC control range.

2.3.2 Loop Gain

Adjust the AGC loop gain to match the AGC control sensitivity of your tuner. The TC90512 provides two registers for adjusting the AGC control gain (aagcdv and aggsft) that can be used to compensate for non-linearity in the control sensitivity of the tuner AGC. This can make the responsiveness of AGC roughly constant across the entire control range and stabilize the AGC loop response. Refer to the product specification manual for details.

[Important] If an inappropriate AGC gain is used, AGC control may overshoot and cause the AGC convergence time to become long. Adjust the gain to match the tuner you are using.

3. Terrestrial Digital Reception

3.1 Getting and Setting the Transmission Mode

Although the TC90512 automatically detects the transmission control information (TMCC) defined by the ISDB-T transmission protocol, the synchronization time when selecting a channel can be made shorter by presetting the TMCC register if the receiver already has this information. It is also possible to preset the mode and guard ratio in the same way.

The registers and their setting values are described below. The initial register values are the following transmission parameters that were in use at the time this application note was written. You do not need to preset the registers if using the same transmission parameters.

TV system, Mode 3, guard ratio = 1/8
Level A: Partial reception 1 segment QPSK, convolution encoding rate CR=1/2, I=4
Level B: 12 segment 64QAM, convolution encoding rate CR=3/4, I=4
Level C: None

Name	Address (HEX)	Data	R/W	Initial Value	Description
mdetsel	47	[7]	W	0x0	Selects whether or not to perform a mode search at the initial lock-on for demodulation 0: Perform mode search at the initial lock-on 1: Do not perform mode search at the initial lock-on However, a mode search is performed when re-locking on.
ffsize [1:0]	B0	[7:6]	R/W	0x2	FFT size monitor output (mode decision output and setting value) 0: 2048 (Mode1) 1: 4096 (Mode2) 2: 8192 (Mode3) 3: Undefined
gdleng [1:0]	B0	[5:4]	R/W	0x2	Guard length monitor output (guard ratio decision output and setting value) 0: 1/32 1: 1/16 2: 1/8 3: 1/4
sysid [1:0]	B2	[7:6]	R/W	0x0	TMCC system identifier 0: TV 1: Audio Other value: Reserved
pachg [3:0]	B2	[5:2]	R/W	0xF	TMCC parameter switching index F: Normal Other value: Number of switching frames - 1
emeflg	B2	[1]	R/W	0x0	TMCC activation flag for emergency warning broadcast 0: No activation control 1: Use activation control
part	B2	[0]	R/W	0x1	TMCC partial reception flag In TV mode: 0: No partial reception 1: Partial reception In audio mode: 0: 1 segment 1: 3 segment
a_cnst [2:0]	B3	[7:5]	R/W	0x1	TMCC level A Carrier modulation protocol 0: DQPSK 1: QPSK 2: 16QAM 3: 64QAM 7: Not hierarchical Other values: Reserved
a_rate [2:0]	B3	[4:2]	R/W	0x1	TMCC level A Convolution encoding rate 0: 1/2 1: 2/3 2: 3/4 3: 5/6 4: 7/8 7: Not hierarchical Other values: Reserved
a_ileav [2:0]	B3	[1:0]	R/W	0x3	TMCC level A Time interleaving For MODE 1 0: I=0 1: I=4 2: I=8 3: I=16 4: I=32 7: Not hierarchical Other values: Reserved

	B4	[7]			For MODE 2 0: I=0 1: I=2 2: I=4 3: I=8 4: I=16 7: Not hierarchical Other values: Reserved For MODE 3 0: I=0 1: I=1 2: I=2 3: I=4 4: I=8 7: Not hierarchical Other values: Reserved
a_seg [3:0]	B4	[6:3]	R/W	0x1	Number of segments used for level A F: Not hierarchical
b_cnst [2:0]	B4	[2:0]	R/W	0x3	TMCC level B Carrier modulation protocol 0: DQPSK 1: QPSK 2: 16QAM 3: 64QAM 7: Not hierarchical Other values: Reserved
b_rate [2:0]	B5	[7:5]	R/W	0x2	TMCC level B Convolution encoding rate 0: 1/2 1: 2/3 2: 3/4 3: 5/6 4: 7/8 7: Not hierarchical Other values: Reserved
b_ileav [2:0]	B5	[4:2]	R/W	0x2	TMCC level B Time interleaving MODE 1 0: I=0 1: I=4 2: I=8 3: I=16 4: I=32 7: Not hierarchical Other values: Reserved MODE 2 0: I=0 1: I=2 2: I=4 3: I=8 4: I=16 7: Not hierarchical Other values: Reserved MODE 3 0: I=0 1: I=1 2: I=2 3: I=4 4: I=8 7: Not hierarchical Other values: Reserved
b_seg [3:0]	B5 B6	[1:0] [7:6]	R/W	0xC	Number of segments used for level B F: Not hierarchical
c_cnst [2:0]	B6	[5:3]	R/W	0x7	TMCC level C Carrier modulation protocol 0: DQPSK 1: QPSK 2: 16QAM 3: 64QAM 7: Not hierarchical Other values: Reserved
c_rate [2:0]	B6	[2:0]	R/W	0x7	TMCC level C Convolution encoding rate 0: 1/2 1: 2/3 2: 3/4 3: 5/6 4: 7/8 7: Not hierarchical Other values: Reserved
c_ileav [2:0]	B7	[7:5]	R/W	0x7	TMCC level C Time interleaving MODE 1 0: I=0 1: I=4 2: I=8 3: I=16 4: I=32 7: Not hierarchical Other values: Reserved MODE 2 0: I=0 1: I=2 2: I=4 3: I=8 4: I=16 7: Not hierarchical Other values: Reserved MODE 3 0: I=0 1: I=1 2: I=2 3: I=4 4: I=8 7: Not hierarchical Other values: Reserved
c_seg [3:0]	B7	[4:1]	R/W	0xF	Number of segments used for level C F: Not hierarchical
phcomp [2:0]	B7 B8	[0] [7:6]	R/W	0x7	Phase correction for concatenated transmission 0: $-\pi/8$ 1: $-2\pi/8$ 2: $-3\pi/8$ 3: $-4\pi/8$ 4: $-5\pi/8$ 5: $-6\pi/8$ 6: $-7\pi/8$ 7: No correction

3.2 Channel Search

A high-speed channel search can be performed using the automatic transmission mode (mode and guard ratio) detection function and synchronization detection function of the TC90512.

3.2.1 Performing a High-Speed Search Using SP Synchronization

Figure 3-1 shows an example of a channel search procedure that determines whether or not an OFDM signal is present.

You can detect whether the OFDM signal is present by checking whether register fulock = 0. By setting mlocksel = 1, the fulock flag changes from a frame synchronization flag to an SP detection flag. As a result, an OFDM signal channel can be identified quickly without waiting for frame synchronization. In this case, however, you cannot also obtain the TMCC which is transmitted synchronized with the frame.

As fulock does not go to 0 if no OFDM signal is present, or if the reception conditions are poor to the point that synchronization cannot occur, this can be used to determine that no OFDM signal is present (or, at least, no OFDM signal capable of being received). It is also possible to improve the detection reliability by using the number of synchronization lock retries as an indication. The retry overflow flag (retryov=1) is output when the number of synchronization lock retries reaches the value set in the retrycnt register. For example, if retrycnt is set to 2, retryov goes to 1 after the second attempt to lock is unable to achieve synchronization. Using retryov = 1 as an indication that no OFDM signal is present is a very reliable method. However, the detection time increases in proportion to the number of retries. Under normal reception conditions it is adequate to use retryov = 1 as the check condition with retrycnt = 1 (that is, first fulock = 0 detection).

3.2.2 Getting TMCC While Searching

Figure 3-2 shows an example of a channel search procedure that gets the TMCC as well as determining whether or not an OFDM signal is present.

It is also possible to detect the OFDM signal at synchronization sequence complete (seqen = 8), the same as in the TC90A87. In this case, do not set mlocksel = 1. Although TMCC can also be obtained because frame synchronization detection is performed during the search, the search time is long compared to the SP synchronization method described in (1).

Whichever of these two methods is used, the mode and guard ratio can be obtained by reading the ffsize and gdleng registers after fulock goes to 0. If fulock is used as the frame synchronization flag, always set mlocksel = 0 after the channel search finishes.

Name	Address (HEX)	Data	R/W	Initial Value	Description
imsrst	01	[6]	W	0x0	Demodulation reset 0: Normal 1: Reset
retrycnt [3:0]	3B	[7:4]	W	0x3	Threshold for detecting when the maximum number of synchronization lock reties has been exceeded retryov=1 is output when the number of retries is greater than the value set here.
retryov	80	[7]	R	0xX	Flag indicating abnormal number of synchronization lock retries The abnormal condition is output when the number of retries is greater than the setting. 0: Normal 1: Invalid (retry limit exceeded)
tmunvld	80	[5]	R	0xX	TMCC not detected flag 0: Detected 1: Not detected
fulock	80	[3]	R	0xX	Frame sync lost flag 0: Synchronized 1: Not synchronized

ffsize [1:0]	B0	[7:6]	R/W	0x0	FFT size monitor output (mode indication output and setting value) 0: 2048 (Mode1) 1: 4096 (Mode2) 2: 8192 (Mode3) 3: Undefined
gdleng [1:0]	B0	[5:4]	R/W	0x0	Guard length monitor output (guard ratio decision output and setting value) 0: 1/32 1: 1/16 2: 1/8 3: 1/4
seqen [3:0]	B0	[3:0]	R/W	0x0	Status information for synchronization sequence 0: Transmission mode detection 1: Initial lock on FFT window position 2: Carrier AFC coarse synchronization 3: Carrier AFC fine synchronization/Clock AFC (gain #1) 4: Carrier AFC fine synchronization/Clock AFC (gain #2) 5: Clock PLL (gain #1) 6: Clock PLL (gain #2) 7: Clock PLL (gain #3) 8: Waiting for FFT window search to complete 9: Synchronization sequence complete

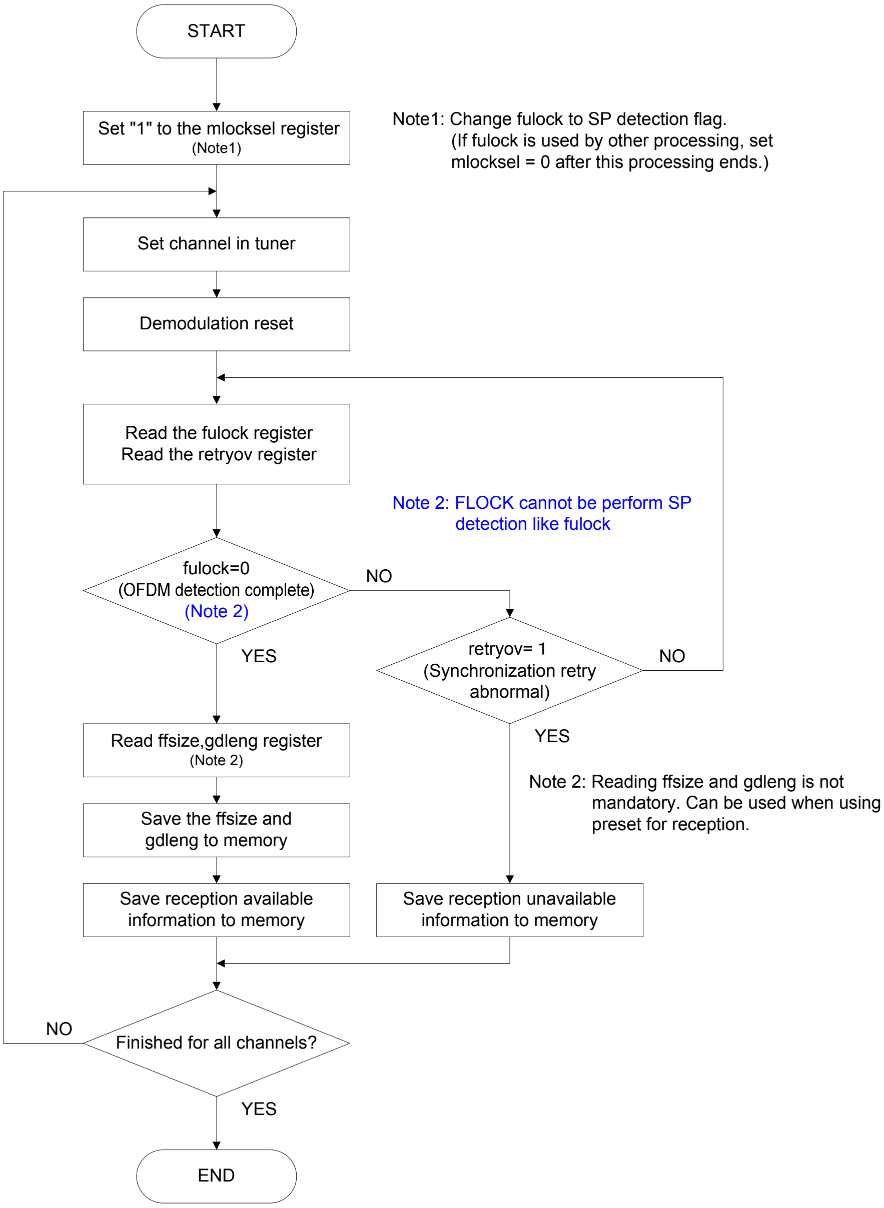


Figure 3-1 Flow Chart for OFDM Channel Search

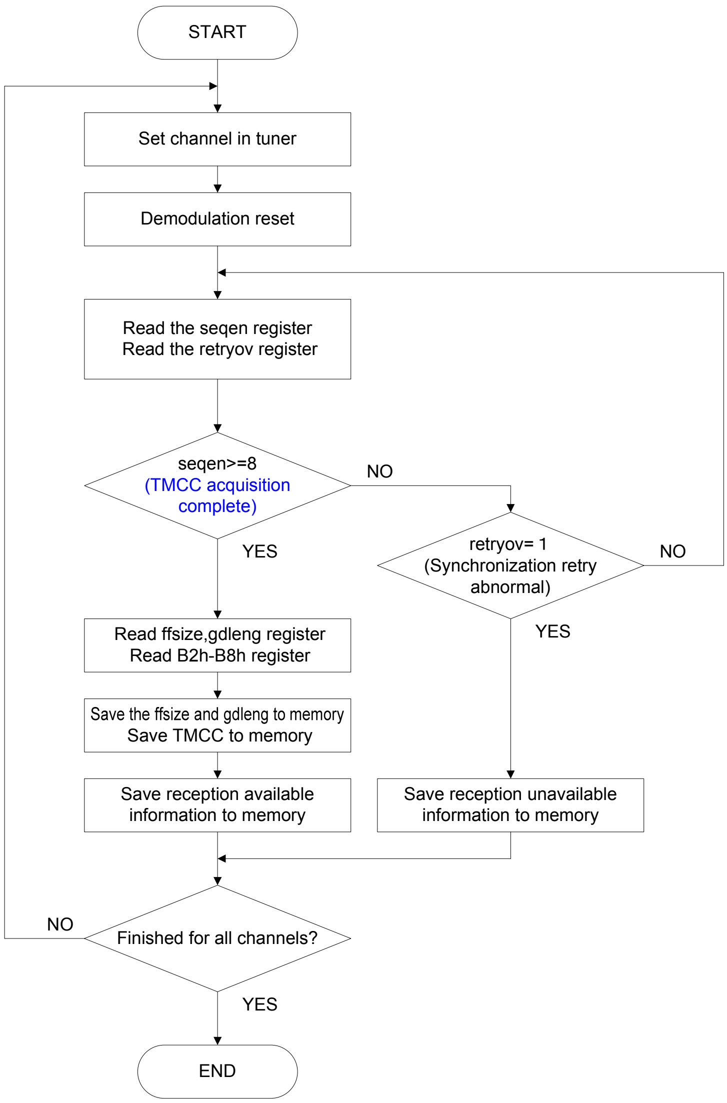


Figure 3-2 Flowchart of Channel Search That Obtains TMCC

3.3 Channel Selection

3.3.1 Presetting the Transmission Mode

Figure 3-3 shows an example channel selection procedure using a preset transmission mode.

Setting register mdetsel = 1 causes the initial synchronization lock to be performed using the transmission mode and guard ratio set in the ffsize and gdleng registers. If the initial lock attempt is unable to achieve synchronization because the received signal uses a different transmission mode to that specified, the second and subsequent lock attempts perform a mode search automatically.

3.3.2 Presetting TMCC

Presetting TMCC is recommended to improve the performance of high-speed channel selection.

As described in section 3.1, the most commonly used transmission parameters are already used as the initial values for the TMCC setting registers (addresses B2h to B8h) on the TC90512, so these do not normally need to be set. However, because it is possible that other transmission parameters specified by operational restrictions may also be used, you should preset the TMCC values from the previously received channel before performing channel selection.

Also, presetting the monitor value from the eqqdt register in the eqqth register can reduce the time required to obtain error free TS. When the TMCC initial values are used as the transmission parameters, error-free TS can be output after 300ms (typ.). Perform this in conjunction with TMCC presetting.

[Important] The time taken to obtain error-free TS can be significantly shortened by writing (presetting) the value read from eqqdt to eqqth when presetting TMCC.

3.3.3 TS Error Free Criteria

The above procedure shortens the time until error-free TS output, and in some cases error-free TS will occur before the standard criteria (FLOCK flag (fulock) and seqen = 8 or 9) are satisfied. Accordingly, instead of these flags, you should use RLOCK (in terms of registers, the OR of rlocka, rlockb, rlockc) which monitors TS error-free directly to determine when demodulation is complete.

[Important] **To identify the error-free condition quickly**, use RLOCK (in terms of registers, the OR of rlocka, rlockb, rlockc) instead of fulock=0 to determine when error-free reception has started.

Note that the time until error-free TS occurs may be longer depending on the mode and guard ratio, time interleave length, and other receive conditions. As demodulation does not start until after TMCC is obtained if the TMCC preset values (or TMCC initial values if not preset) are different to the received signal, this will result in a longer time until error-free TS.

If partial receive level A is multiplexed, the time until consecutive error-free TS can be determined will be longer because level A has a low rate, and the time interleave may also be longer. Accordingly, if receiving level B only, it is necessary to exclude level A from the TS error-free criteria. In this case, it is not possible to use rulock (goes to 0 when no errors on any level) instead of the above RLOCK.

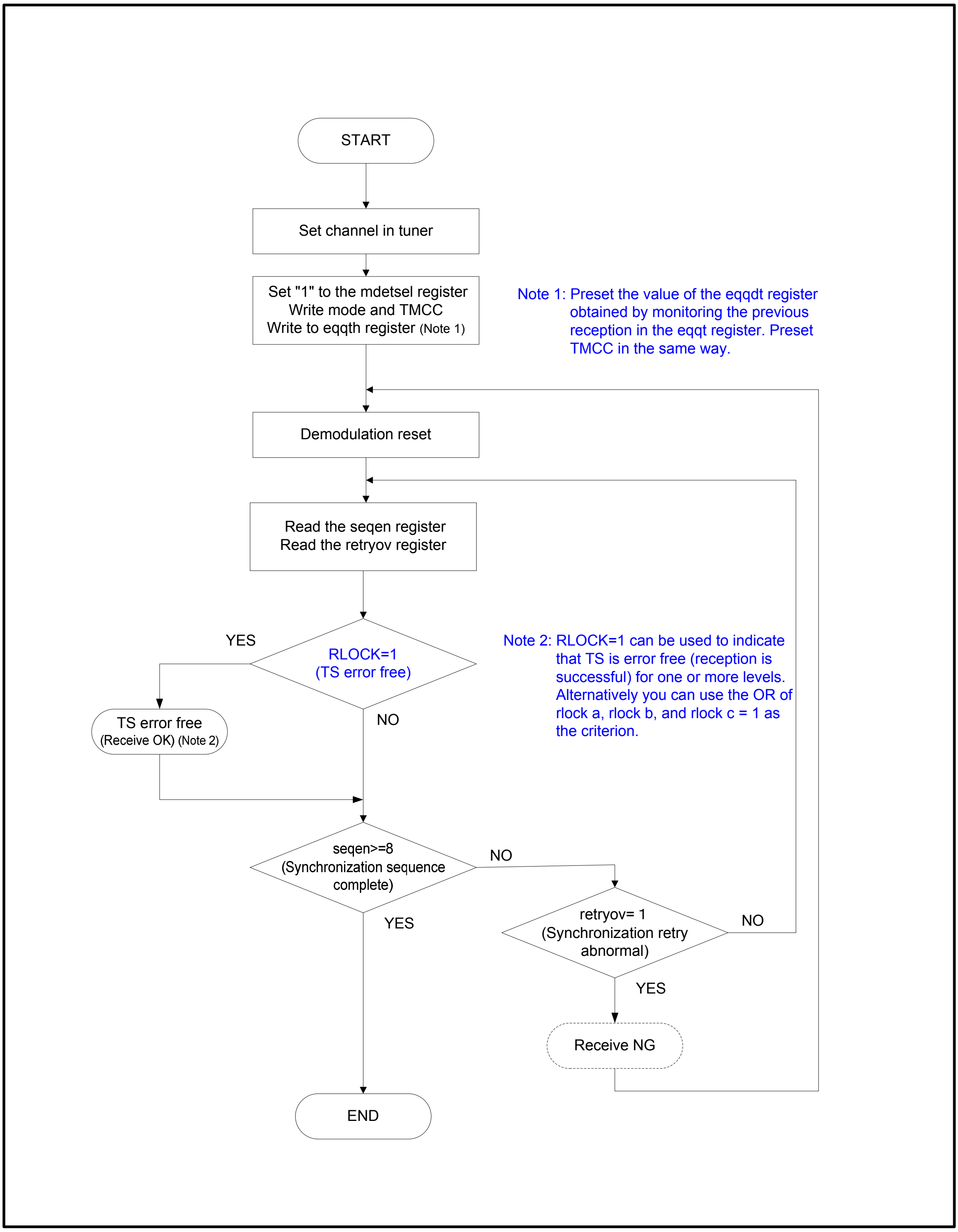


Figure 3-3 Flowchart for OFDM Channel Selection

3.4 Circuit for Canceling Interference Between Multi-Path Symbols (ISIC)

The TC90512 includes an inter-symbol interference canceller (ISIC) circuit to suppress multi-path interference outside the guard range. The maximum delay time that can be cancelled is -250μs to +250μs and this improves the out-of-guard multi-path D/U ratio by 0 to 5dB for 64QAM 3/4.

The default setting for the ISIC is off. Performing an imsrst demodulation reset with sydfmd = "1" turns the circuit on. When turned on, the ISIC operates automatically based on the input conditions.

Setting ISIC on is ignored for 3/1 segment or a 1/4 guard ratio. The same applies if a differential segment is included. Similarly, the ISIC cannot operate at the same time as the FFT window continuous control function. When the ISIC is enabled, only the FFT window search during demodulation reset is performed. However, if no out-of-guard multi-path is present, ISIC halts automatically and FFT window continuous control is used.

[Important] The default setting for ISIC is off, but turning the circuit on improves the multi-path characteristics. Although the FFT window continuous search is not performed when ISIC is operating, ISIC is halted automatically and FFT window continuous control performed if no out-of-guard multi-path is present.

3.5 Narrow-Band Reception

3.5.1 Setting the Operating Mode

The TC90512 can decode narrow-band (3 or 1 segment) OFDM signals for terrestrial digital audio broadcasting by setting the recvmd[1:0] register. The tuner output for the band corresponding to the number of segments is input as the IF signal when receiving, and a 1 segment OFDM signal can be received on a 3 segment tuner.

Name	Address (HEX)	Data	R/W	Initial Value	Description
recvmd [1:0]	02	[7:6]	W	0x0	Receive segment mode selection 0: TV reception (13 segment) 2: Audio reception (1 segment) 3: Audio reception (3 segment)
segsel [3:0]	02	[3:0]	W	0x0	Sets the central segment for audio reception 0 to 13
recvmdsel	EC	[3]	W	0x0	Receive mode selection for 3 segment reception 0: 3 segment fixed 1: Auto-select 1 segment or 3 segment

1) Receive 13 segment TV broadcast signal on 13 segment band:
   recvmd = 0
2) Receive partial reception level for TV broadcast on 13 segment band:
   recvmd = 0 (Set laysel=3 to specify null packet for other than level A)
3) Receive 3 or 1 segment audio broadcast signal on 3 segment band:
   recvmd = 3, segsel = Center segment number, recvmdsel = 1
4) Receive 1 segment audio broadcast signal on 1 segment band:
   recvmd = 2, segsel = Center segment number

3.5.2 Digital Tuning

For the case of receiving a 1 segment OFDM signal on a 3 segment band tuner (case 3), set the station frequency on the tuner such that the segment to be received is at the center of the SAW filter (3 segment bandwidth).

If the segment to be received is at the edge of the channel band, however, there is a risk that an adjacent analog TV channel overlaps the tuner's filter band. In this case, the 1 segment OFDM signal at the edge of the channel can be demodulated by performing digital tuning with the tuner station frequency shifted by one segment (that is, shift the center frequency of the filter away from the channel center by one segment so that the analog TV signal no longer overlaps).

As digital tuning will demodulate the signal with the input IF frequency shifted, adjust the value in the cpld_dt register by an amount equivalent to a +3/7MHz shift in the IF frequency (corresponding to 1 segment band). This allows demodulation of the OFDM segment shifted up or down by one segment from the original IF center frequency. In this case, leave segsel set to its original value.

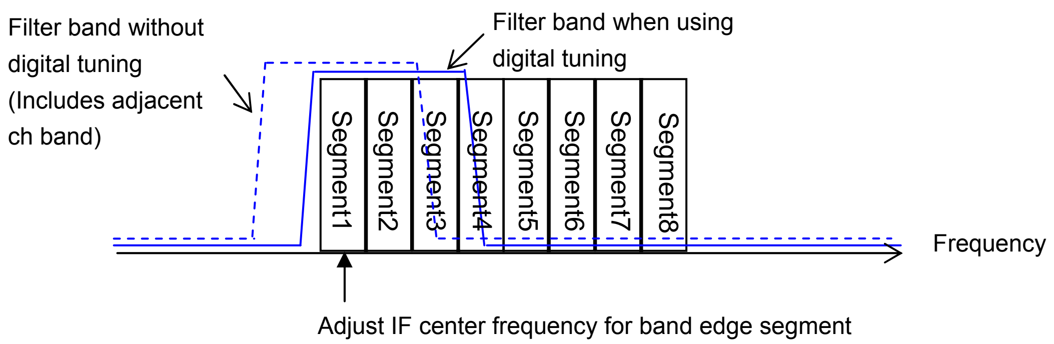


Figure 3-4 Example of Digital Tuning on a 3 Segment Tuner

3.6 AGC Control

Some of the AGC control register settings need to be modified to match the tuner you are using. Example settings are described below.

3.6.1 AGC Limiter Setting

The AGC limiter function is used when the characteristics of the AGC amplifier are such that saturation can occur. The function can be used to prevent a sudden reduction in AGC control sensitivity and deterioration of control response in the region where saturation occurs.
Use the rf_max and rf_min registers to set the upper and lower limits respectively for the RF_AGC control range. Similarly, use the if_max and delayp registers to set the upper and lower limits respectively for the IF_AGC control range.

3.6.2 Loop Gain

Adjust the RF_AGC loop gain (rfagcg1 and rfagcg2) and IF_AGC loop gain (ifagcg1 and ifagcg2) to match the AGC control sensitivity of your tuner. In both cases, different gains can be set for lock-on and normal operation.
The gain for lock-on should be set higher to speed up the channel selection time. The gain for normal operation should be set lower to prevent AGC control from becoming unstable due to static or phasing.
As the syini_tim register is also provided to specify how long to delay the start of demodulation to allow AGC lock-on to complete, ensure that AGC lock-on completes within this wait time.
The TC90512 can compensate for non-linearity in the control sensitivity of the tuner AGC to make the responsiveness of AGC roughly constant across the entire control range and stabilize the AGC loop response. Refer to the product specification manual for details.

3.6.3 Delay Point Setting

The delay point for RF_AGC/IF_AGC switching control mode (configuration whereby both control signals are returned to the tuner) can be set in the delayp register.

3.6.4 Using S_INFO for AGC Adaptive Control

If a tuner distortion detection output is available, this can be input to the S_INFO to allow AGC control to operate with an adaptive delay point. (The tuner distortion detection output must output a "1" if the distortion up to the IFAGC stage exceeds the threshold.) Refer to section 9.7.5 of the product specification manual for details of control operation.

3.6.5 Initial Values for AGC Control

The following are the initial values for AGC control after a demodulation reset in RF_AGC/IF_AGC switching control mode.

- RF_AGC initial value: rf_max setting value
- IF_AGC initial value: delayp setting value

The following are the initial values for AGC control after a demodulation reset in IF_AGC control mode

- IF_AGC initial value: ifmgc setting value (with delayp as the lower limit)

The standard settings for reliable operation are ifmgc = 80h and delayp = 00h.

Note that the initial value registers for IF-AGC are different in each mode.
To reduce the AGC convergence time, set AGC control values suitable for normal reception conditions as the initial values.

[Important] To reduce the AGC convergence time, set an appropriate AGC initial value and loop gain.

3.7 Adaptive FFT Window Search

The TC90512 can maintain good reception even for multi-path by performing an automatic search for the FFT window position. The FFT window search starts automatically when a system reset or demodulation reset occurs.

In addition to the initial search after a reset, the TC90512 continues to search continuously while demodulation is in progress, Accordingly, even if the input conditions change, performing a reset or similar is not required. However, this does not include the case when ISIC is turned on and is suppressing out-of-guard multi-path interference.

3.8 Adaptive Pilot Interpolation Filter

The pilot interpolation filter on the TC90512 automatically selects optimum control for time interpolation and frequency interpolation in accordance with their respective input conditions. The optimization of the frequency interpolation filter, in particular, has flexible required D/U characteristics up to +/-250μs for both pre and post-echo for 1/8 guard. (If the ISIC is enabled, the required D/U ratio can be improved by up to about 15dB.)

Note that, adaption for pilot interpolation is controlled inside the IC and therefore does not require external software control.

3.9 Improving the Characteristics for Multi-Path

The TC90512 has a number of circuits for suppressing carrier interference. One of these is the PLR circuit which estimates the carrier interference from the variation in modulating wave spectrum and interpolates the damaged pilot. However, because the PLR uses changes in the frequency direction of the spectrum as its reference, it is likely to misoperate under bad multi-path conditions.

Although the default register setting turns the PLR circuit on, considering multi-band and multi-path, it is recommended to turn PLR off under normal receive conditions. The deterioration in the required D/U ratio with respect to analog TV interference in this case is very small at only 0.5dB.

To turn PLR circuit off: Address 5Fh Change from 00h (initial value) to 80h

Revision History

2006/07/14	rev.001	Initial document	
2006/08/17	rev.002	2.1	Added settings for 52h, 53h, 5Ah, and 5Bh registers in PSK unit
		3.4	Corrected note relating to ISIC
		3.6.5	Added "Initial Values for AGC Control" section
2006/08/18	rev.100	2.1	Added settings for 51h, 52h, 53h, 5Ah, and 5Bh registers
2006/09/13	rev.101	3.3.1	Deleted explanation of mmode
2006/12/12	rev.102	2.1	Changed/added explanation of psksyrst=1 in PSK unit initialization
2007/03/05	rev.103	3.9	Changed to recommend turning PLR circuit off