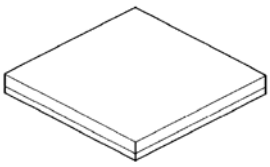
Toshiba CMOS Digital Integrated Circuit Silicon Monolithic

TC90512XBG

Demodulation and error correction for Japanese Integrated Services Digital Broadcasting Satellite and Terrestrial receivers

TC90512XBG is a Japanese Integrated Services Digital Broadcasting Satellite (ISDB-S) and Digital Broadcasting Terrestrial (ISDB-T) system compliant IC that performs demodulation and error correction.
The input signal is an orthogonal detector baseband signal for digital satellite demodulation and an orthogonal detector baseband signal or 4 MHz and 57 MHz intermediate frequency (IF) band signal for digital terrestrial demodulation. The output signal is a demodulated and error-corrected MPEG-2 transport signal.
This IC can accommodate to all transmission modes and parameters of both transmission systems, and perform demodulation and error correction of both systems simultaneously.



P-FBGA177-1313-0.80C4

Weight: 0.39 g (Standard)

Features

- **Digital satellite (ISDB-S) demodulation and error correction**
  - Built-in AD converter compliant with differential/single ended input
  - Built-in adaptive phase noise tracking circuit
  - Built-in adaptive waveform equalizer
  - Built-in de-interleave memory
  - Built-in IQ orthogonal deviation correction and IQ gain correction circuit
  - AGC control output
  - LNB control tone output
  - High-speed channel switching possible
- **Digital terrestrial (ISDB-T) demodulation and error correction**
  - All 2k/4k/8k carrier modes and 3-layered transmission, including partial reception, supported
  - 3/1 segment narrow band ISDB-T, including linked transmission, compatible
  - Transmission mode (number of carriers/guard period) automatic detection
  - IQ baseband signal or 4 MHz/57 MHz IF signal input possible
  - Built-in AD converter compliant with differential/single ended input
  - Built-in unguarded multipath canceler (ISIC) compliant with SFN
  - Continuous control of FFT window position possible
  - Built-in tuner phase noise suppressing circuit and co-channel interference suppressing circuit
  - RF/IF independent AGC control output
  - Built-in digital AGC and AFC circuit
  - Built-in tuner AGC adaptive control circuit
  - Built-in digital filter
  - High-speed channel switching and channel search possible
- **Common**
  - Stand-alone operation possible
  - Crystal oscillation output pin
  - Built-in C/N monitor, error rate monitor, and constellation monitor functions
  - MPEG-2 transport stream output (parallel or serial output)
  - I^2C control pin for fast mode (400 kHz) I^2C compatible tuner
  - Standby operation compatible with emergency alarm broadcast startup possible (satellite and terrestrial independent control)
  - JTAG boundary scan supported
  - Compact 177-pin PFBGA package (13 mm x 13 mm x 1.4 mm)
  - 1.2 V, 2.5 V power supply voltage (I/O area: 3.3 V)
  - Low power consumption 310 mW (simultaneous satellite/terrestrial demodulation typ.)
  - Operating ambient temperature: -20 to +85°C

- 90 nm CMOS process

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* **Notation in red characters (the color used in the history of changes) indicates changes along with the version up.**

<About the peripheral circuits in this document>

The peripheral circuits referred to in this document are only an example of means of evaluation of the operation of this product. They are neither intended for recommendation or standardization of peripheral circuit configuration or constants nor used for mass production of application systems. (This is because system characteristics differ with the externally installed parts used by the customer, packaging patterns, and other conditions.)
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1. Overview of TC90512XBG Features

1.1 Digital Satellite (PSK) Demodulation and Error Correction

1) ISDB-S mode compliant

- BS digital signals in ISDB-S transmission mode and CS digital signals in wide-band 110° mode can be demodulated. (DVB-S mode for narrow-band CS is not supported.)

2) Built-in AD converter

- The IC has a built-in AD converter that is differential input compatible.
- 0.375 Vp-p (differential voltage 0.75 Vp-p) differential input or 0.75 Vp-p single-ended input are supported.

3) Built-in adaptive phase noise tracking circuit

- The IC controls the PLL loop gain adapting to the change of C/N and modulation combinations and tracks LNB phase noise, thereby performing stabilized high-precision carrier recovery control.

4) Pull-in of carrier and clock frequencies

- Carrier frequencies in the range of ±5 MHz and clock frequencies in the range of ±200 ppm or more can be pulled in.

5) Built-in adaptive waveform equalizer

- The IC has a built-in adaptive waveform equalizer that automatically equalizes waveform distortion caused by cable reflection.

6) IQ axis gain deviation/orthogonal deviation correction circuit

- The IC automatically corrects the amplitude deviation and orthogonal deviation of IQ baseband input signals.
- The amplitude deviation can be corrected in the range of ±2 dB and the orthogonal deviation in the range of ±5°.

7) Built-in tone signal generation circuit for LNB control

- Tone signal generation for LNB control is possible.

8) High-speed channel switching

- Demodulation output in a short time is possible even under low C/N conditions.
- Demodulation synchronization is possible in approximately 100 ms if 8PSK reception is possible.

1.2 Digital Terrestrial (OFDM) Demodulation and Error Correction

1) Built-in AD converter

- The IC has a built-in wide-band AD converter. IF signals of 57 MHz can be input directly.
- 0.5 Vp-p (differential voltage 1.0 Vp-p) differential input or 1.0 Vp-p single-ended input are supported.

2) Built-in memory

- The system contains all of the necessary memory for signal processing. The memory required for time de-interleaving is also built-in, rendering external memory installation unnecessary.

3) IF and IQ baseband signal input supported

- Low IF signals with a center frequency of 4 MHz, 44 MHz, or 57 MHz can be input directly.
- Orthogonal detected IQ baseband signals can be input instead of IF input signals. In the case if IQ input, the IC automatically corrects the amplitude deviation and orthogonal deviation of IQ inputs.

5) All ISDB-T modes supported

- The system supports all transmission modes and transmission parameters specified in the ISDB-T transmission scheme.
- Three carrier number count modes, four guard ratios, three-layered transmission, four modulation methods, five convolution encoding rates, and all time de-interleave lengths are supported.
- One- or three-segment narrow band ISDB-T (ISDB-T_{SB}) are also supported.
- Reception in narrow-band ISDB-T linked transmission mode is also possible.

6) Phase noise suppressing circuit

- A tuner phase noise suppressing circuit is contained.

7) Pull-in of carrier and clock frequencies

- Carrier frequencies in the range of ±250 kHz and clock frequencies in the range of ±200 ppm or more can be pulled in.

8) Adaptive pilot interpolation circuit

- An optimum frequency or time filter interpolation characteristics are selected according to input conditions.
- C/N is improved under the conditions in which no fading occurs, while some improvement is recognized even under the conditions that involves multipath delay or analogue TV interferences. On the other hand, time tracking characteristics are held under the conditions with fading.

9) Adaptive FFT window position control

- The position of the FFT window is controlled constantly and automatically for the maximum demodulation S/N.
- Multipath with a positive or negative delay time generated from SFN (single frequency network), including the guard ratio of 1/4, is also supported.

10) Built-in unguarded multipath canceler (ISIC)

- The IC has a built-in circuit that suppresses intersymbol interferences generated by multipaths that exceed the guard period
- Multipath interferences with a delay time up to 250 μs at the guard ratio of 1/8 in Mode 3 are suppressed

11) Adaptive error control

- Interferences such as terrestrial transmission channel multipath interferences and carrier interferences with different properties are analyzed (CSI and CVI) to control error correction adaptively.
- The IC has a built-in circuit to suppress analog TV interferences of the same channel.
- The system uses an algorithm to cope with high-speed time fluctuation, thereby coping with phasing such as fluttering as well.

12) High-speed channel search

- This function can determine presence or absence of OFDM signals in a short time, thereby making it possible to perform channel search at a higher speed. The time of determining presence or absence of signals is approximately 0.2 s per channel.
- During channel search, the OFDM signal mode and guard ratio are automatically detected. This information can be preset as well.

13) High-speed channel switching

- The parallel processing by demodulation synchronization and efficient initialization function permit the TS output to be obtained at the time of channel switching in a brief period (300 ms typ.).
- Presetting of mode or guard ratio and TMCC is possible, allowing the TS output time to be shortened. If the preset values are incorrect, no external control is required since they are corrected automatically.

14) RF/IF independent and adaptive AGC control

- RF and IF AGC control signals are output from respective independent terminals.

- The AGC delay control can be set digitally.
- The IC can usually be used as a single AGC control. In that case, the RF AGC control output can be used as a generalized DC voltage control output.
- The IC can provide an adaptive delay control by inputting distortion signals from the tuner
- Input or output through the AGC control signals (digital) from other demodulating IC is possible

15) Digital filter and digital AGC

- The IC has a built-in digital filter to suppress adjacent analog TV interferences.
- It also has a built-in digital AGC circuit that is useful for low-level input and out-of-band interference input.
- With the digital tuning function, demodulation of any segment of 3- or 1-segment OFDM signals is possible without changing the tuner station frequency.

1.3 Common Functions

1) Satellite/Terrestrial independent I^2C control

- Different I^2C slave addresses are used for digital satellite demodulationand digital terrestrial demodulation. As a result, TC90512XBG can be handled as if two independent ICs are controlled from the outside.
- Readable/writable tuner I^2C through control pins are provided independently for satellite and terrestrial.
- Fast mode (400 kHz) I^2C is supported.

2) Satellite/Terrestrial independent TC output

- TS outputs for digital satellite demodulation and digital terrestrial demodulation are independently provided.
- MPEG transport stream can be output in parallel or serial format. It is possible to output the stream in both formats at the same time.

3) BER monitor

- The bit error rate (BER) after Viterbi correction or Reed-Solomon correction can be monitored via the I^2C bus.
- The measurement cycle can be specified by frames or by packets.

4) S/N monitor

- The deviation of the constellation (complex vector of digital modulation) from the specified value can be calculated and the S/N of the demodulation signal can be read via the I^2C bus.
- The S/N monitor values are independent of the modulation scheme. The S/N monitor is helpful for antenna adjustment since it permits measurements in a briefer time compared with BER measurement.
- S/N monitoring less affected by carrier interference is possible.

5) External control not required (stand-alone operation)

- Basic functions and operations are implemented only in the IC-contained circuits.
- The parameters of the ISDB-S and ISDB-T transmission modes are automatically set by the built-in TMCC demodulator.

6) Standby operation

- Digital satellite demodulation and digital terrestrial demodulation are each standby operational. Power consumption can be saved by operating only those functions to be used.
- Even when both are simultaneously operated, power consumption as low as 310 mW (typ.) can be achieved.
- Both digital satellite demodulation and digital terrestrial demodulation support automatic startup control of emergency alarm broadcasting.

7) Compact package

- TC90512XBG is a 177-pin BGA package.
- The IC can easily be packaged with a ball pitch of 0.8 mm. The package is as small as 13 mm x 13 mm x 1.4 mm.

8) Others

- TC90512XBG is provided with status registers and flags useful for interrupt control. (Various flags can be output at change points.)
- Each pin can be enabled or disabled independently. Unnecessary pins can be used as general-purpose output ports.
- Assignment of the TS output pins can be changed. IC boards with proper pin assignment can be used.
- Clock regeneration can be performed with no VCXO (voltage control crystal oscillator). Operation is possible only on crystal clocks or external reference clocks. External reference clocks are supplied through low-amplitude input pins (0.5 - 2.5 Vp-p).
- The reset pins and I^2C pins are 5V-tolerant. When the TC90512XBG power supply is cut off, these pins have high impedance.
- TC90512XBG is provided with output pins to supply the crystal oscillator output to the outside. When multiple demodulation ICs are used at the same time, the crystal can be shared by those ICs.
- JTAG boundary scan is supported.
- The sequence of power on and off need not be specified.

2. Configuration

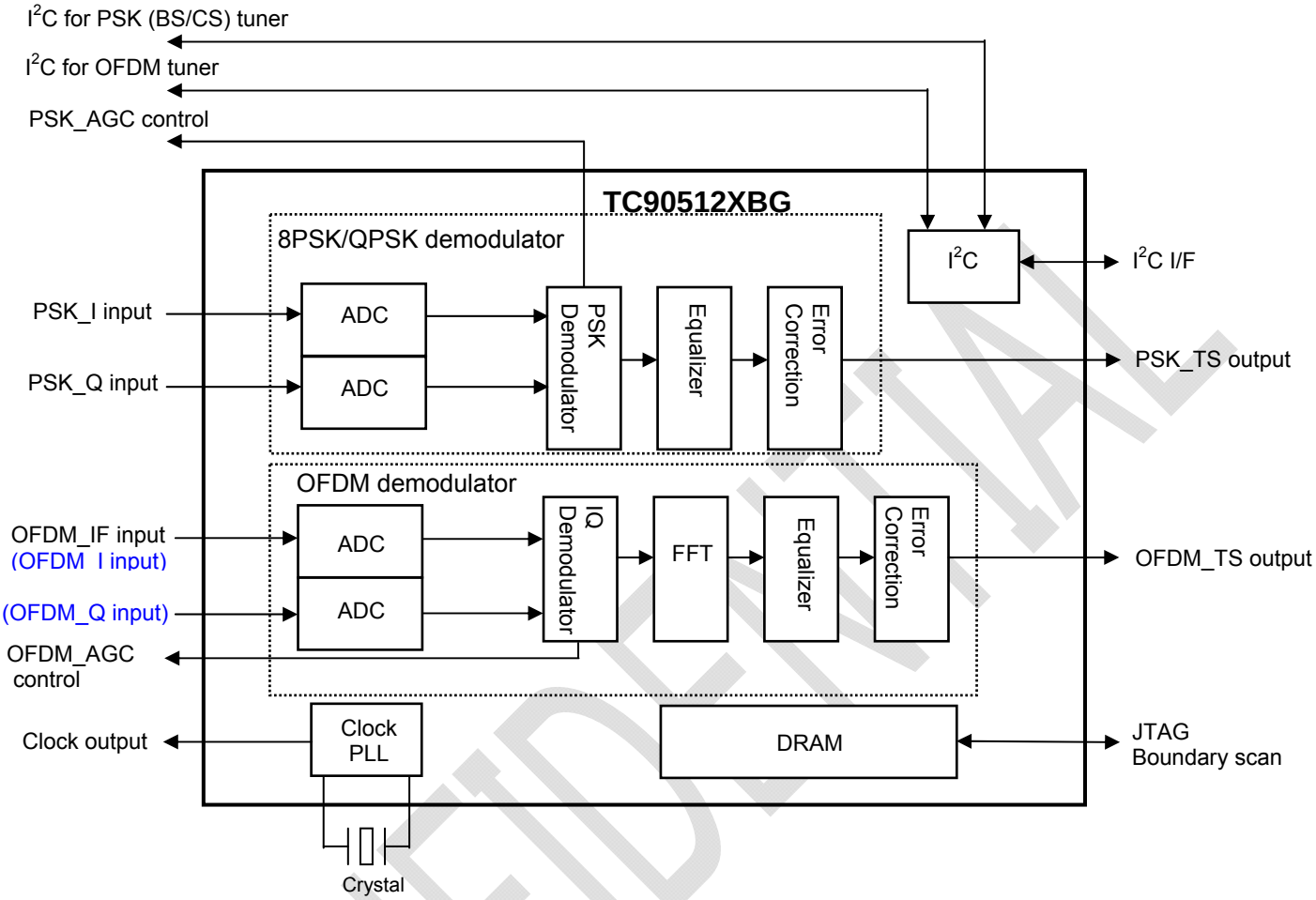
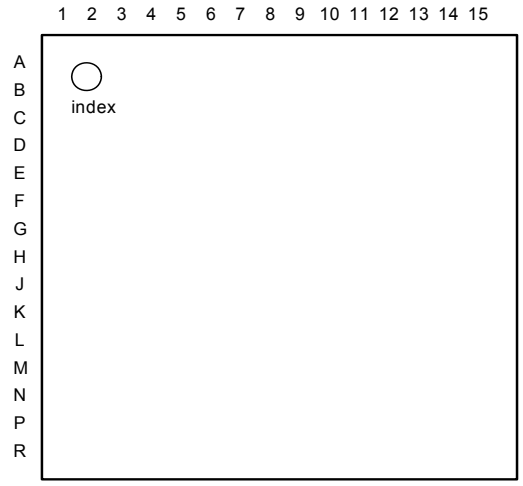


Fig. 2.1 Function Block Diagram

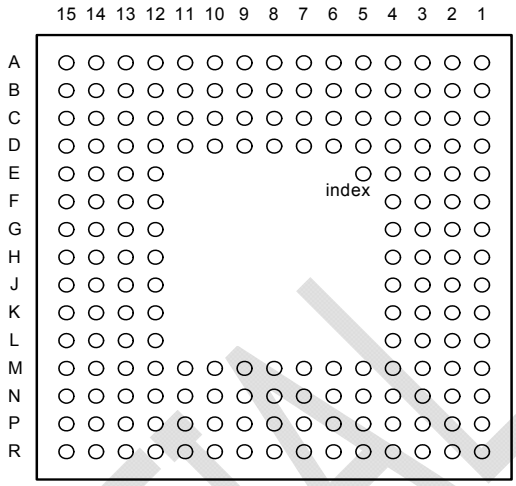
- The PSK demodulator and the OFDM demodulator are independently operational. TS output is also independently provided.
- The PSK demodulator and the OFDM demodulator are controlled by switching the slave address of the I^2C register. As a result, TC90512XBG can be handled as if two independent ICs are controlled from the outside.
- The PSK demodulator and the OFDM demodulator can be placed in the sleep status independently by the standby function, for saving power when they are not used.
- Both of the PSK demodulator and the OFDM demodulator assume the demodulating status in their initial status. Place individual demodulator in the standby mode by the sleep function as needed. (Resetting of the register is not required when either demodulator is restored from the standby more.)

3. Pin Assignment

(This pin assignment is not compatible with TC90502XBG.)



Top View



Bottom View

Pin Name List

	1	2	3	4	5	6	7	8
A	MDO	TDI	TMS	JSRCK	JRSCKO	JPBVAL	JSTSFLG1	JLOCK
B	TCK	TRST	JOEN	JSRDT	JSBYTE	JRSEORF	JSTSFLG0	JPORT
C	JRSOUT7	JRSOUT6	TSMD3	VDDS	VDDC	VDDS	TESI5	VDDC
D	JRSOUT5	JRSOUT4	DTMB	VSS	VSS	VSS	VSS	VSS
E	JRSOUT3	JRSOUT2	VDDS	VSS	NC (INDEX)			
F	JRSOUT1	JRSOUT0	VDDC	VSS				
G	JRLOCKH	JRLOCKL	VDDC	VSS				
H	SLADRS1	SLADRS0	VDDS	VSS				
J	XSEL1	XSEL0	VDDC	VSS				
K	XCKOSL	EXTCK	VDDC	VSS				
L	JAGCCNT	TSMD2	VDDS	VSS				
M	JTNSCL	JTNSDA	VDDC	VSS	NC	NC	NC	NC
N	JLNB	JAD_DVDD	JAD_LVDD	JAD_LVSS	NC	NC	NC	PLLVSS
P	JAD_DVSS	JAD_AVDD	JAD_AVSS	JAD_AVSS	NC	NC	XOVSS	XOVDD
R	NC	JADI_AIP	JADI_AIN	JADQ_AIP	JADQ_AIN	JAD_VCM	XCKO	XO

	9	10	11	12	13	14	15
A	SRCK	RSCKO	PBVAL	STSFLG1	FLOCK	TDO	FSO
B	SRDT	SBYTE	RSEORF	STSFLG0	SLPEN	CKI	SYRSTN
C	TSMD1	VDDS	VDDC	TSMD0	TESI4	SDA	SCL
D	VSS	VSS	VSS	VSS	DR2VDD	RSOUT6	RSOUT7
E				DR1VDD	VDDS	RSOUT4	RSOUT5
F				VSS	VDDC	RSOUT2	RSOUT3
G				VSS	DR1VDD	RSOUT0	RSOUT1
H				VSS	VDDS	RERR	RLOCK
J				VSS	DR1VDD	TESI3	OEN
K				VSS	VDDC	TESI2	TESI1
L				VSS	VDDS	TESI0	S_INFO
M	NC	AD_CM	AD_VREFN	VSS	DR1VDD	TNSDA	AGCI
N	VDDC	AD_DVSS	AD_VREF	AD_VREFP	VDDC	AGCCNTI	TNSCL
P	PLLVDD	AD_DVDD	NC	AD_AVSS	AD_AVDD	VDDS	AGCCNTR
R	XI	FIL	ADI_AIP	ADI_AIN	ADQ_AIP	ADQ_AIN	DTCLK

4. Pin Functions

(This pin assignment is not compatible with TC90502XBG.)

In this specification, **pins and their signals are indicated in upper case,** and I^2C **registers and their signals in lower case**.

XSEL1 No.	Pin name (Note 2)	(Note 5) I/O	(Note 6) PU/PD	(Note 1) Class	Function	Remarks (Notes 3, 4, and 7)
A1	MDO	O	–	–	Pin for pre-shipment test	Open because fixed to L in normal operation.
A2	TDI	I	PU	–	JTAG data input	Open when JTAG not used.
A3	TMS	I	PU	–	JTAG mode setting	Open when JTAG not used.
A4	JSRCK	O	–	PSK	TS serial clock output	Open, fixed to L when not used.
A5	JRSCKO	O	–	PSK	TS byte clock output	Open, fixed to L when not used.
A6	JPBVAL	O	–	PSK	TS valid flag output	Open, fixed to L when not used.
A7	JSTSFLG1	O	–	PSK	Status flag 1 output	Open, fixed to L when not used.
A8	JLOCK	O	–	PSK	Super frame sync	Open, fixed to L when not used.
A9	SRCK	O	–	OFDM	TS serial clock output	Open, fixed to L when not used.
A10	RSCKO	O	–	OFDM	TS byte clock output	Open, fixed to L when not used.
A11	PBVAL	O	–	OFDM	TS valid flag output	Open, fixed to L when not used.
A12	STSFLG1	O	–	OFDM	Status flag 1 output	Open, fixed to L when not used.
A13	FLOCK	O	–	OFDM	Frame synchronization flag output	Open, fixed to L when not used.
A14	TDO	O	–	–	JTAG data output	Open when JTAG not used.
A15	FSO	O	–	–	Pin for pre-shipment test	Open because fixed to L in normal operation.
B1	TCK	I	–	–	JTAG clock output	Connects to DGND when JTAG is not used.
B2	TRST	I	–	–	JTAG reset output	Connects to DGND when JTAG is not used.
B3	JOEN	I	PD	PSK	Output pin disable control input	0: Enable, 1: Disable
B4	JSRDT	O	–	PSK	Serial TS data output	Open, fixed to L when not used.
B5	JSBYTE	O	–	PSK	TS synchronization byte flag output	Open, fixed to L when not used.
B6	JRSEORF	O	–	PSK	TS error flag output	Open, fixed to L when not used.
B7	JSTSFLG0	O	–	PSK	Status flag 0 output	Open, fixed to L when not used.
B8	JPORT	O	–	PSK	General-purpose port output (Or LNB power supply control output)	Open, fixed to L when not used.
B9	SRDT	O	–	OFDM	Serial TS data output	Open, fixed to L when not used.
B10	SBYTE	O	–	OFDM	TS synchronization byte flag output	Open, fixed to L when not used.
B11	RSEORF	O	–	OFDM	TS error flag output	Open, fixed to L when not used.
B12	STSFLG0	O	–	OFDM	Status flag 0 output	Open, fixed to L when not used.
B13	SLPEN	O	–	OFDM	Sleep status flag output	Open, fixed to L when not used.
B14	CKI	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
B15	SYRSTN	I/O	–	–	System reset input	Input at specified timing at power ON.
C1	JRSOUT7	I/O (Note 5)	PD	PSK	TS parallel data 7 output	Open, fixed to L when not used.
C2	JRSOUT6	I/O (Note 5)	PD	PSK	TS parallel data 6 output	Open, fixed to L when not used.
C3	TSMD3	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
C4	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
C5	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
C6	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
C7	TESI5	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
C8	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
C9	TSMD1	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
C10	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
C11	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
C12	TSMD0	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
C13	TESI4	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.

C14	SDA	I/O	–	–	I^2C data I/O for host CPU	Connects to ^2C data bus (Pull-up performed outside IC.)
C15	SCL	I/O(Note 5)	–	–	I^2C clock input for host CPU	Connects to I^2C clock bus (Pull-up performed outside IC.)
D1	JRSOUT5	I/O(Note 5)	PD	PSK	TS parallel data 5 output	Open, fixed to L when not used.
D2	JRSOUT4	I/O(Note 5)	PD	PSK	TS parallel data 4 output	Open, fixed to L when not used.
D3	DTMB	I	PU	–	Pin for pre-shipment test	Open or connects to digital +3.3 V typ.
D4	VSS	–	–	–	Digital GND	Connects to DGND.
D5	VSS	–	–	–	Digital GND	Connects to DGND.
D6	VSS	–	–	–	Digital GND	Connects to DGND.
D7	VSS	–	–	–	Digital GND	Connects to DGND.
D8	VSS	–	–	–	Digital GND	Connects to DGND.
D9	VSS	–	–	–	Digital GND	Connects to DGND.
D10	VSS	–	–	–	Digital GND	Connects to DGND.
D11	VSS	–	–	–	Digital GND	Connects to DGND.
D12	VSS	–	–	–	Digital GND	Connects to DGND.
D13	DR2VDD	–	–	–	Digital power supply	Connects to digital +2.5 V typ.
D14	RSOUT6	O	–	OFDM	TS parallel data 6 output	Open, fixed to L when not used.
D15	RSOUT7	O	–	OFDM	TS parallel data 7 output	Open, fixed to L when not used.
E1	JRSOUT3	I/O(Note 5)	PD	PSK	TS parallel data 3 output	Open, fixed to L when not used.
E2	JRSOUT2	I/O(Note 5)	PD	PSK	TS parallel data 2 output	Open, fixed to L when not used.
E3	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
E4	VSS	–	–	–	Digital GND	Connects to DGND.
E5	NC (INDEX)	–	–	–	Not connected	Not connected to chip.
E12	DR1VDD	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
E13	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
E14	RSOUT4	O	–	OFDM	TS parallel data 4 output	Open, fixed to L when not used.
E15	RSOUT5	O	–	OFDM	TS parallel data 5 output	Open, fixed to L when not used.
F1	JRSOUT1	I/O(Note 5)	PD	PSK	TS parallel data 1 output	Open, fixed to L when not used.
F2	JRSOUT0	I/O(Note 5)	PD	PSK	TS parallel data 0 output	Open, fixed to L when not used.
F3	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
F4	VSS	–	–	–	Digital GND	Connects to DGND.
F12	VSS	–	–	–	Digital GND	Connects to DGND.
F13	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
F14	RSOUT2	O	–	OFDM	TS parallel data 2 output	Open, fixed to L when not used.
F15	RSOUT3	O	–	OFDM	TS parallel data 3 output	Open, fixed to L when not used.
G1	JRLOCKH	I/O(Note 5)	PD	PSK	High layer RS error free flag output	Open, fixed to L when not used.
G2	JRLOCKL	I/O(Note 5)	PD	PSK	Low layer RS error free flag output	Open, fixed to L when not used.
G3	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
G4	VSS	–	–	–	Digital GND	Connects to DGND.
G12	VSS	–	–	–	Digital GND	Connects to DGND.
G13	DR1VDD	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
G14	RSOUT0	O	–	OFDM	TS parallel data 0 output	Open, fixed to L when not used.
G15	RSOUT1	O	–	OFDM	TS parallel data 1 output	Open, fixed to L when not used.
H1	SLADRS1	I	PD	–	Slave address 1	Set according to slave address.
H2	SLADRS0	I	PD	–	Slave address 0	Set according to slave address.
H3	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
H4	VSS	–	–	–	Digital GND	Connects to DGND.
H12	VSS	–	–	–	Digital GND	Connects to DGND.
H13	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
H14	RERR	O	–	OFDM	RS decoding error flag output	Open, fixed to L when not used.
H15	RLOCK	O	–	OFDM	RS decoding error free flag output	Open, fixed to L when not used.

J1	XSEL1	I	PD	–	Crystal frequency division ratio 1	Set according to crystal frequency.
J2	XSEL0	I	PD	–	Crystal frequency division ratio 0	Set according to crystal frequency.
J3	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
J4	VSS	–	–	–	Digital GND	Connects to DGND.
J12	VSS	–	–	–	Digital GND	Connects to DGND.
J13	DR1VDD	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
J14	TESI3	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
J15	OEN	I	PD	OFDM	Output pin disable control input	0: Enable, 1: Disable
K1	XCKOSL	I	PD	–	Crystal oscillation output control	0: Enable, 1: Disable
K2	EXTCK	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
K3	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
K4	VSS	–	–	–	Digital GND	Connects to DGND.
K12	VSS	–	–	–	Digital GND	Connects to DGND.
K13	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
K14	TESI2	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
K15	TESI1	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
L1	JAGCCNT	I/O(Note 5)	PD	PSK	AGC control output	Connects to tuner AGC control input.
L2	TSMD2	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
L3	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
L4	VSS	–	–	–	Digital GND	Connects to DGND.
L12	VSS	–	–	–	Digital GND	Connects to DGND.
L13	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
L14	TESI0	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.
L15	S_INFO	I	PD	OFDM	Delay point adaptive control input (Tuner distortion signal input)	Effective when sifon=1 Open or connects to DGND when not used.
M1	JTNSCL	I/O(Note 5)	–	PSK	I2C clock output	Connects to tuner I2C clock pin. (Pull-up performed outside IC.)
M2	JTNSDA	I/O	–	PSK	I2C data I/O	Connects to tuner I2C data pin. (Pull-up performed outside IC.)
M3	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
M4	VSS	–	–	–	Digital GND	Connects to DGND.
M5	NC	–	–	–	Not connected	Not connected to chip.
M6	NC	–	–	–	Not connected	Not connected to chip.
M7	NC	–	–	–	Not connected	Not connected to chip.
M8	NC	–	–	–	Not connected	Not connected to chip.
M9	NC	–	–	–	Not connected	Not connected to chip.
M10	AD_CM	–	–	OFDM	ADC reference voltage output	+1.25 V typ. Connects to AGND via PC, and also connects to AD_VREF.
M11	AD_VREFN	–	–	OFDM	ADC reference voltage output	+0.75 V typ. Connects to AGND via PC.
M12	VSS	–	–	–	Digital GND	Connects to DGND.
M13	DR1VDD	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
M14	TNSDA	I/O	–	OFDM	I2C data I/O	Connects to tuner I2C data pin. (Pull-up performed outside IC.)
M15	AGCI	I	PD	OFDM	External AGC input	Open or connects to DGND when not used.
N1	JLNB	I/O(Note 5)	PD	PSK	LNB control output	Open or connects to DGND when not used.
N2	JAD_DVDD	–	–	PSK	ADC digital power supply	Connects to digital +2.5 V typ.
N3	JAD_LVDD	–	–	PSK	ADC digital power supply	Connects to analog +1.2 V typ.(Note 8)
N4	JAD_LVSS	–	–	PSK	ADC digital GND	Connects to AGND.
N5	NC	–	–	–	Not connected	Not connected to chip.
N6	NC	–	–	–	Not connected	Not connected to chip.
N7	NC	–	–	–	Not connected	Not connected to chip.
N8	PLLVSS	–	–	–	Clock PLL GND	Connects to AGND.
N9	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.

N10	AD_DVSS	–	–	OFDM	ADC digital GND	Connects to DGND.
N11	AD_VREF	–	–	OFDM	ADC reference voltage input	Connects to AD_CM.
N12	AD_VREFP	–	–	OFDM	ADC reference voltage output	+1.75 V typ. Connects to AGND via PC.
N13	VDDC	–	–	–	Digital power supply	Connects to digital +1.2 V typ.
N14	AGCCNTI	I/O(Note 5)	PD	OFDM	IF_AGC control output	Connects to tuner IF_AGC control input pin.
N15	TNSCL	I/O(Note 5)	–	OFDM	I2C clock output	Connects to tuner I2C clock pin. (Pull-up performed outside IC.)
P1	JAD_DVSS	–	–	PSK	ADC digital GND	Connects to DGND.
P2	JAD_AVDD	–	–	PSK	ADC analog power supply	Connects to analog +2.5 V typ.
P3	JAD_AVSS	–	–	PSK	ADC analog GND	Connects to AGND.
P4	JAD_AVSS	–	–	PSK	ADC analog GND	Connects to AGND.
P5	NC	–	–	–	Not connected	Not connected to chip.
P6	NC	–	–	–	Not connected	Not connected to chip.
P7	XOVSS	–	–	–	Crystal oscillation GND	Connects to AGND.
P8	XOVDD	–	–	–	Crystal oscillation power supply	Connects to analog +2.5 V typ.
P9	PLLVDD	–	–	–	Clock PLL power supply	Connects to analog +2.5 V typ.
P10	AD_DVDD	–	–	PSK	Digital power supply	Connects to digital +2.5 V typ.
P11	NC	–	–	–	Not connected	Not connected to chip.
P12	AD_AVSS	–	–	OFDM	ADC analog GND	Connects to AGND.
P13	AD_AVDD	–	–	OFDM	ADC analog power supply	Connects to analog +2.5 V typ.
P14	VDDS	–	–	–	I/O power supply	Connects to digital +3.3 V typ.
P15	AGCCNTR	I/O(Note 5)	**PD**	OFDM	RF_AGC control output	Connects to tuner RF_AGC control input pin. Open, fixed to L when not used.
R1	NC	–	–	–	Not connected	Not connected to chip.
R2	JADI_AIP	I	–	PSK	I signal (differential positive side) input	Connects to tuner I (+) output after DC decoupling.
R3	JADI_AIN	I	–	PSK	I signal (differential negative side) input	Connects to tuner I (-) output after DC decoupling. Connects to AGND via PC when not used.
R4	JADQ_AIP	I	–	PSK	Q signal (differential positive side) input	Connects to tuner Q (+) output after DC decoupling.
R5	JADQ_AIN	I	–	PSK	Q signal (differential negative side) input	Connects to tuner Q (-) output after DC decoupling. Connects to AGND via PC when not used.
R6	JAD_VCM	–	–	PSK	ADC reference voltage output	Connects to AGND via +1.25 V typ. PC.
R7	XCKO	O	–	–	Crystal oscillation output	Open and output OFF when not used.
R8	XO	O	–	–	Crystal output	Connects to crystal.
R9	XI	I	–	–	Crystal output	Connects to crystal.
R10	FIL	O	–	–	Clock PPL filter output	Connects to AGND via 1500pF.
R11	ADI_AIP	I	–	OFDM	IF signal (differential positive side) input, or I signal (differential positive side) input	Connects to tuner IF (+) output after DC decoupling, or connects to tuner I (+) output.
R12	ADI_AIN	I	–	OFDM	IF signal (differential negative side) input, or I signal (differential negative side) input	Connects to tuner IF (-) output after DC decoupling, or connects to tuner I (-) output.
R13	ADQ_AIP	I	–	OFDM	Q signal (differential positive side) input	Connects to AGND via PC, or connects to tuner Q (+) output.
R14	ADQ_AIN	I	–	OFDM	Q signal (differential negative side) input	Connects to AGND via PC, or connects to tuner Q (-) output.
R15	DTCLK	I	PD	–	Pin for pre-shipment test	Open or connects to DGND.

Note 1) PSK refers to a digital satellite demodulation dedicated pin, and OFDM refers to a digital terrestrial demodulation dedicated pin. All other pins are commonly used. (**The digital satellite dedicated pin names begin with J.**)
Note 2) NC unused pins are not connected to the chip.
Note 3) AGND indicates analog GND, and DGND indicates digital GND.

Note 4) The test dedicated pin is used for the pre-shipment test only. Be sure processing is performed as indicated in the "Remarks" column.
Any other method will lead to malfunction or failure.

Note 5) I/O indicates the type of the cell used. It may be different from the pin function because a test is conducted concurrently.

Note 6) PU indicates an I/O with a pull-up resistor (50 kΩ typ.) and PD indicates an I/O with a pull-down resistor (50 kΩ typ.). Pulling down or up the respective resistance outside the IC sometimes changes the electric potential to the midpoint, resulting in instability. Caution is required.

Note 7) The reserved output pins must be fixed to L by setting the control register of each pin for noise reduction or set to the output OFF state.

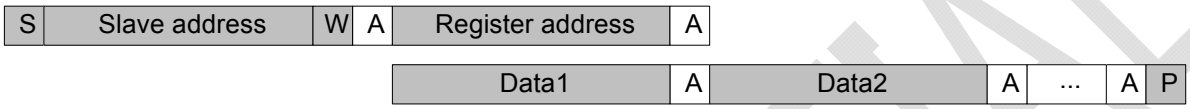
Note 8) When a digital 1.2 V power supply is used, implement isolation by a coil.

5. Host CPU Interface

5.1 I²C Bus Interface

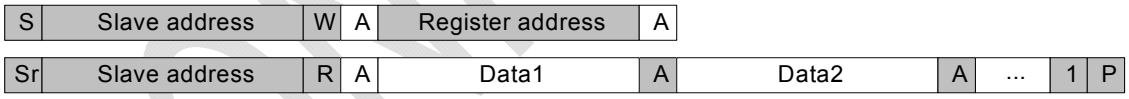
The I²C bus is used as the interface with the host CPU. It can read and write data to and from registers.When the LSB of a slave address is "0," it reads or writes data to or from the registers of the **digital terrestrial (OFDM)** demodulator and error correction circuit. When the LSB of a slave address is "1," it reads or writes data to or from the registers of the **digital satellite (PSK)** demodulator and error correction circuit.
Through-write mode and through-read mode allow you to perform read and write operations against the I²C register of the digital terrestrial or BS/CS tuner IC via TC90512.
The highest operating frequency of the I²C bus clock is 400 kHz.

(1) Write mode



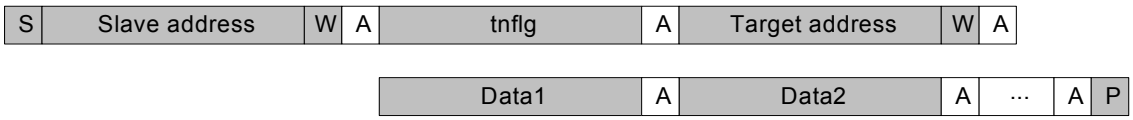
S	Start condition	
Slave address	I²C address	"0011"+SLADRS1+SLADRS0 +"0"(7bit) : OFDM
		"0011"+SLADRS1+SLADRS0 +"1"(7bit) : PSK
R/W	0:write 1:read	
A	Acknowledge	
Register address	Start address (8bit)	
Data1,2,...	Write data (8bit)	
P	Stop condition	
■	from master to slave	
□	from slave to master	

(2) Read mode



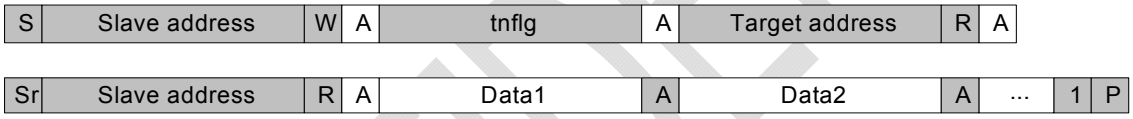
S	Start condition	
Slave address	I²C address	"0011"+SLADRS1+SLADRS0 +"0"(7bit) : OFDM
		"0011"+SLADRS1+SLADRS0 +"1"(7bit) : PSK
R/W	0:write 1:read	
A	Acknowledge	
Register address	Start address (8bit)	
Data1,2,...	Read data (8bit)	
P	Stop condition	
Sr	Repeated start	
■	from master to slave	
□	from slave to master	

(3) Through-write mode



S	Start condition	
Slave address	I^2C address	"0011"+SLADRS1+SLADRS0+"0"(7bit) : OFDM
		"0011"+SLADRS1+SLADRS0+"1"(7bit) : PSK
R/W	0:write 1:read	
A	Acknowledge	
tnflg address	through start address (11111110)	
Target address	target slave address (7bit)	
Data1,2,...	Write data (8bit)	
P	Stop condition	
	from master to slave	
	from slave to master	

(4) Through-read mode



S	Start condition	
Slave address	I^2C address	"0011"+SLADRS1+SLADRS0+"0"(7bit) : OFDM
		"0011"+SLADRS1 +SLADRS0 +"1"(7bit) : PSK
R/W	0:write 1:read	
A	Acknowledge	
tnflg address	through start address (11111110)	
Target address	target slave address (7bit)	
Data1,2,...	Read data (8bit)	
P	Stop condition	
Sr	Repeated start	
	from master to slave	
	from slave to master	

[Important] In through-write mode and through-read mode, usage that lengthens the bus clock low period of the TNSCL and JTNSCL pins is not permitted. (Although this type of function is included in I^2C specifications, TC90512 through modes do not support it.)

5.2 Register Address Map

5.2.1 PSK Demodulation Register Map

Address [HEX]	Data (upper section)/Initial value (lower section)								Initial Value [HEX]	R/W
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
01	psksyrst								10	W
	0	0	0	1	0	0	0	0		
03								pskmsrst	00	W
	0	0	0	0	0	0	0	0		
04				emgmsk			chclkp		00	W
	0	0	0	0	0	0	0	0		
06		iqch			bytesel	jhselout			00	W
	0	0	0	0	0	0	0	0		
07		jtsld		jtslc		jtslb		jtsla	41	W
	0	1	0	0	0	0	0	1		
09	aglmin[7:0]								00	W
	0	0	0	0	0	0	0	0		
0A	aglmax[7:0]								FF	W
	1	1	1	1	1	1	1	1		
0C	jhkfrq[15:8]								XSEL	W
	-	-	-	-	-	-	-	-		
0D	jhkfrq[7:0]								XSEL	W
	-	-	-	-	-	-	-	-		
0E						agcgn[2:0]			F0	W
	1	1	1	1	0	0	0	0		
0F	afcg[7:0]								XSEL	W
	-	-	-	-	-	-	-	-		
10			aagcdv[2:0]				amglvl[9:8]		B2	W
	1	0	1	1	0	0	1	0		
11	amglvl[7:0]								00	W
	0	0	0	0	0	0	0	0		
12	aagpcw[1:0]		aggsft[1:0]		aggthr[3:0]				30	W
	0	0	1	1	0	0	0	0		
13	jslpadc	atpt	jslpmd						00	W
	0	0	0	0	0	0	0	0		
14		lnb	jport						00	W
	0	0	0	0	0	0	0	0		
15				tetim[4:0]					00	W
	0	0	0	0	0	0	0	0		
17	watim[7:0]								00	W
	0	0	0	0	0	0	0	0		
1A	inpnone	unlocke	crslipe	tmcerre	sdivee	rlockle	tmcreve	tmchge	00	W
	0	0	0	0	0	0	0	0		
1B	inpnoneiv	unlockeiv	crslipeiv	tmcerreiv	sdiveeiv	rlockleiv	tmcreveiv	tmchgeiv	00	W
	0	0	0	0	0	0	0	0		
1C	bpbv_en[1:0]		brse_en[1:0]		bstf1_en[1:0]		bstf0_en[1:0]		00	W
	0	0	0	0	0	0	0	0		
1D	bstat_en[1:0]		block_en[1:0]		bstatl_en[1:0]		brso_en[1:0]		00	W
	0	0	0	0	0	0	0	0		
1E			bpot_en[1:0]		bagc_en[1:0]				00	W
	0	0	0	0	0	0	0	0		
1F	blnb_en[1:0]		bsrf_en[1:0]		brsck_en[1:0]		bsby_en[1:0]		00	W
	0	0	0	0	0	0	0	0		
20	jstmdd[1:0]		jstmdc[1:0]		jstmdb[1:0]		jstmda[1:0]		00	W
	0	0	0	0	0	0	0	0		
38	acolvl[7:0]								40	W
	0	1	0	0	0	0	0	0		

39	aagref[7:0]								10	W
	0	0	0	1	0	0	0	0		
3B								deqoff	90	W
	1	0	0	1	0	0	0	0		
51	pllhmax[3:0]								C0	W
	1	1	0	0	0	0	0	0		
52							pllbhgd[5:4]		8A	W
	1	0	0	0	1	0	1	0		
53	pllbhgd[3:0]								13	W
	0	0	0	1	0	0	1	1		
57	tston								00	W
	0	0	0	0	0	0	0	0		
5A							pllqhgd[5:4]		2E	W
	0	0	1	0	1	1	1	0		
5B	pllqhgd[3:0]								23	W
	0	0	1	0	0	0	1	1		
85			adfs[1:0]						59	W
	0	1	0	1	1	0	0	1		
87						aagcinv			00	W
	0	0	0	0	0	0	0	0		
8D	rsoff	tmoff	msboff		nullon_h	nullon_l	tmccadd		00	W
	0	0	0	0	0	0	0	0		
8E	hlmask[1:0]		dvaloff		beron	pkstop	nuval	valrev	00	W
	0	0	0	0	0	0	0	0		
8F	iits[15:8]								00	W
	0	0	0	0	0	0	0	0		
90	iits[7:0]								00	W
	0	0	0	0	0	0	0	0		
A3	anuval	cych[2:0]			asyncng	cycl[2:0]			77	W
	0	1	1	1	0	1	1	1		
A4	rsckrev	shch[2:0]				shcl[2:0]			00	W
	0	0	0	0	0	0	0	0		
A5	tschh	corchh						jperst	00	W
	0	0	0	0	0	0	0	0		
A6		erval[2:0]			oponff	okval[2:0]			04	W
	0	0	0	0	0	1	0	0		
B8	tsic[15:8]								00	R
	0	0	0	0	0	0	0	0		
B9	tsic[7:0]								00	R
	0	0	0	0	0	0	0	0		
BA	crunlock	agcmc[6:0]							00	R
	0	0	0	0	0	0	0	0		
BB	afcfrq[7:0]								00	R
	0	0	0	0	0	0	0	0		
BC	cnmc[15:8]								00	R
	0	0	0	0	0	0	0	0		
BD	cnmc[7:0]								00	R
	0	0	0	0	0	0	0	0		
BE	clkfrq[7:0]								00	R
	0	0	0	0	0	0	0	0		
C3	inpnon	unlock	crslip	tmcerr	sdive	emgcy	tmcrev	tmchg	00	R
	0	0	0	0	0	0	0	0		
C5	pm1d[4:0]						rlockh	rlockl	00	R
	0	0	0	0	0	0	0	0		
C6	acnt[5:0]								00	R
	0	0	0	0	0	0	0	0		
C7					uplink[3:0]				00	R
	0	0	0	0	0	0	0	0		

C8	d_mode1[3:0]				d_mode2[3:0]				00	R
	0	0	0	0	0	0	0	0		
C9	d_mode3[3:0]				d_mode4[3:0]				00	R
	0	0	0	0	0	0	0	0		
CA			s_mode1[5:0]						00	R
	0	0	0	0	0	0	0	0		
CB			s_mode2[5:0]						00	R
	0	0	0	0	0	0	0	0		
CC			s_mode3[5:0]						00	R
	0	0	0	0	0	0	0	0		
CD			s_mode4[5:0]						00	R
	0	0	0	0	0	0	0	0		
CE	tsid0[15:8]								00	R
	0	0	0	0	0	0	0	0		
CF	tsid0[7:0]								00	R
	0	0	0	0	0	0	0	0		
D0	tsid1[15:8]								00	R
	0	0	0	0	0	0	0	0		
D1	tsid1[7:0]								00	R
	0	0	0	0	0	0	0	0		
D2	tsid2[15:8]								00	R
	0	0	0	0	0	0	0	0		
D3	tsid2[7:0]								00	R
	0	0	0	0	0	0	0	0		
D4	tsid3[15:8]								00	R
	0	0	0	0	0	0	0	0		
D5	tsid3[7:0]								00	R
	0	0	0	0	0	0	0	0		
D6	tsid4[15:8]								00	R
	0	0	0	0	0	0	0	0		
D7	tsid4[7:0]								00	R
	0	0	0	0	0	0	0	0		
D8	tsid5[15:8]								00	R
	0	0	0	0	0	0	0	0		
D9	tsid5[7:0]								00	R
	0	0	0	0	0	0	0	0		
DA	tsid6[15:8]								00	R
	0	0	0	0	0	0	0	0		
DB	tsid6[7:0]								00	R
	0	0	0	0	0	0	0	0		
DC	tsid7[15:8]								00	R
	0	0	0	0	0	0	0	0		
DD	tsid7[7:0]								00	R
1	0	0	0	0	0	0	0	0		
DE	exfld[60:53]								00	R
	0	0	0	0	0	0	0	0		
DF	exfld[52:45]								00	R
	0	0	0	0	0	0	0	0		
E0	exfld[44:37]								00	R
	0	0	0	0	0	0	0	0		
E1	exfld[36:29]								00	R
	0	0	0	0	0	0	0	0		
E2	exfld[28:21]								00	R
	0	0	0	0	0	0	0	0		
E3	exfld[20:13]								00	R
	0	0	0	0	0	0	0	0		
E4	exfld[12:5]								00	R
	0	0	0	0	0	0	0	0		

E5	exfld[4:0]								00	R
	0	0	0	0	0	0	0	0		
E6	tsido[15:8]								00	R
	0	0	0	0	0	0	0	0		
E7	tsido[7:0]								00	R
	0	0	0	0	0	0	0	0		
E8	nul_h	rateh[2:0]			nul_l	ratel[2:0]			00	R
	0	0	0	0	0	0	0	0		
E9			sloth[5:0]						00	R
	0	0	0	0	0	0	0	0		
EA			slotl[5:0]						00	R
	0	0	0	0	0	0	0	0		
EB	perrh[23:16]								00	R
	0	0	0	0	0	0	0	0		
EC	perrh[15:8]								00	R
	0	0	0	0	0	0	0	0		
ED	perrh[7:0]								00	R
	0	0	0	0	0	0	0	0		
EE	pecyh[15:8]								00	R
	0	0	0	0	0	0	0	0		
EF	pecyh[7:0]								00	R
	0	0	0	0	0	0	0	0		
F0	perrl[23:16]								00	R
	0	0	0	0	0	0	0	0		
F1	perrl[15:8]								00	R
	0	0	0	0	0	0	0	0		
F2	perrl[7:0]								00	R
	0	0	0	0	0	0	0	0		
F3	pecyl[15:8]								00	R
	0	0	0	0	0	0	0	0		
F4	pecyl[7:0]								00	R
	0	0	0	0	0	0	0	0		
FE	tnflg [7:0]								00	W
	0	0	0	0	0	0	0	0		

* The shaded areas indicate unused or test registers. Do not set a value different from the initial value.
* For some registers, a value that differs from the initial value must be set during normal operation as well. (Refer to the evaluation software.)
* Under R/W, "W" indicates a write-only register and "R" indicates a read-only register. Note that the value written in the "W" register can be checked by reading the value from the same register address, excluding the following registers:

  Address 01h Data [7] psksyrst
  Address 03h Data [0] pskmsrst
  Address A5h Data [0] jperst
  Address FEh Data [7:0] tnflg[7:0]

* The registers with XSEL described in their "Initial value" column are set automatically when some or all of them are reset to SYRSTN by the XSEL1 and XSEL0 pins. Bits that are set automatically are indicated by "-".

5.2.2 OFDM Demodulation Register Map

Address [HEX]	Data (upper section)/Initial value (lower section)								Initial Value [HEX]	R/W
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
01	isyrst	imsrst		iwsrst	slpmd	slplkmon			00	W
	0	0	0	0	0	0	0	0		
02	recvmd[1:0]				segsel[3:0]				00	W
	0	0	0	0	0	0	0	0		
03	slpadc	slptim[2:0]			wuptim[3:0]				00	W
	0	0	0	0	0	0	0	0		
04							ixckosl	ixosl	XCKOSL	W
	0	0	0	0	0	0	-	0		
05	stdisa[7:0]								00	W
	0	0	0	0	0	0	0	0		
06	stdisb[7:3]								00	W
	0	0	0	0	0	0	0	0		
07	stinva[7:0]								00	W
	0	0	0	0	0	0	0	0		
08	stinvb[7:3]								00	W
	0	0	0	0	0	0	0	0		
0C	stmda[1:0]		stmdb[1:0]		flmd[1:0]		rlmd[1:0]		00	W
	0	0	0	0	0	0	0	0		
0F	pinsld[1:0]		pinslc[1:0]		pinslb[1:0]		pinsla[1:0]		F4	W
	1	1	1	1	0	1	0	0		
11			ilpdiv[5:0]						XSEL	W
	0	0	-	-	-	-	-	-		
12				iexdiv[4:0]					XSEL	W
	-	-	-	-	-	-	-	-		
13	hkfrq[15:8]								XSEL	W
	0	0	0	0	0	0	0	0		
14	hkfrq[7:0]								XSEL	W
	0	0	0	0	0	0	0	0		
15	hkncog[1:0]								40	W
	0	1	0	0	0	0	0	0		
17	clkg_h[1:0]		clkg_l[1:0]						70	W
	0	1	1	1	0	0	0	0		
18			ckpliwg[2:0]			ckpli1g[2:0]			31	W
	0	0	1	1	0	0	0	1		
19			ckpli2g[2:0]			ckpli3g[2:0]			13	W
	0	0	0	1	0	0	1	1		
1A			ckpldwg[2:0]			ckpld1g[2:0]			31	W
	0	0	1	1	0	0	0	1		
1B			ckpld2g[2:0]			ckpld3g[2:0]			13	W
	0	0	0	1	0	0	1	1		
1C	agccntioen[1:0]		agccntroen[1:0]		stsflg1oen[1:0]		stsflg0oen[1:0]		00	W
	0	0	0	0	0	0	0	0		
1D	rlockoen[1:0]		rerroen[1:0]		rsoutoen[1:0]			hselout	00	W
	0	0	0	0	0	0	0	0		
1E	flockoen[1:0]		slpenoen[1:0]		sroen[1:0]		rsckooen[1:0]		00	W
	0	0	0	0	0	0	0	0		
1F	sbyteoen[1:0]		pbvaloen[1:0]		rseorfoen[1:0]				00	W
	0	0	0	0	0	0	0	0		
20	delayp[7:0]								00	R/W
	0	0	0	0	0	0	0	0		
21	rf_max[7:0]								FF	W
	1	1	1	1	1	1	1	1		
22	rfif	sifon	sifinv	agcthr	agdacnt[1:0]		agdack[1:0]		80	W
	1	0	0	0	0	0	0	0		

23	ifagcg1[2:0]			ifagcg2[2:0]			ifagc_inv	ifmgcon	4C	W
	0	1	0	0	1	1	0	0		
24	rfagcg1[2:0]			rfagcg2[2:0]			rfagc_inv	rfmgcon	4C	W
	0	1	0	0	1	1	0	0		
25	ifmgc[7:0]								00	W
	0	0	0	0	0	0	0	0		
26	rfmgc[7:0]								00	W
	0	0	0	0	0	0	0	0		
27	dpstep[7:0]								0C	W
	0	0	0	0	1	1	0	0		
28	dp_sft				ifthd[3:0]				60	W
	0	1	1	0	0	0	0	0		
29	dplmth[7:0]								6B	W
	0	1	1	0	1	0	1	1		
2A	dplmtl[7:0]								40	W
	0	1	0	0	0	0	0	0		
2B	dpcttim				rfthd[3:0]				40	W
	0	1	0	0	0	0	0	0		
2C	almh[7:0]								FF	W
	1	1	1	1	1	1	1	1		
2D	alml[7:0]								00	W
	0	0	0	0	0	0	0	0		
2E	if_max[7:0]								FF	W
	1	1	1	1	1	1	1	1		
2F	rf_min[7:0]								00	W
	0	0	0	0	0	0	0	0		
30	carg_h[1:0]		carg_l[1:0]		f_inv	sbchlmt			XSEL	W
	0	0	1	0	-	0	0	0		
31			cpld_dt[13:8]						XSEL	W
	0	0	-	-	-	-	-	-		
32	cpld_dt[7:0]								XSEL	W
	-	-	-	-	-	-	-	-		
34			lpfsl[1:0]		ifsch[1:0]		rfsch[1:0]		XSEL	W
	0	0	-	-	1	1	1	1		
38								affrq[8]	XSEL	W
	0	0	0	0	0	0	0	-		
39	affrq[7:0]								XSEL	W
	-	-	-	-	-	-	-	-		
3A	syini_tim[7:0]								10	W
	0	0	0	1	0	0	0	0		
3B	retrycnt[3:0]			symds_off[11:8]					10	W
	0	0	0	1	0	0	0	0		
3C	symds_off[7:0]								00	W
	0	0	0	0	0	0	0	0		
3D	cdtref[7:0]								10	W
	0	0	0	1	0	0	0	0		
3E	ofsref[7:0]								08	W
	0	0	0	0	1	0	0	0		
3F	afctim_1[7:0]								0C	W
	0	0	0	0	1	1	0	0		
40	afctim_2[7:0]								0C	W
	0	0	0	0	1	1	0	0		
41	plltim_1[7:0]								00	W
	0	0	0	0	0	0	0	0		
42	plltim_2[7:0]								00	W
	0	0	0	0	0	0	0	0		
43	fmax_ini[3:0]				fdtmax[3:0]				4F	W
	0	1	0	0	1	1	1	1		

44					ndtmax[3:0]				FF	W
	1	1	1	1	1	1	1	1		
46	tlimsel[1:0]		mgthsel[1:0]						20	W
	0	0	1	0	0	0	0	0		
47	mdetsel	mlocksel							00	W
	0	0	0	0	0	0	0	0		
48	cnth[7:0]								90	W
	1	0	0	1	0	0	0	0		
49	md1_cpd[1:0]		md2_cpd[1:0]		md3_cpd[1:0]				E6	W
	1	1	1	0	0	1	1	0		
4A	syimp_off		wlimsel[1:0]		wslim[2:0]				02	W
	0	0	0	0	0	0	1	0		
4B								syld_off	80	W
	1	0	0	0	0	0	0	0		
4C	tdtmax[1:0]		cpdmax[1:0]		spdmax[1:0]		tmdmax[1:0]		00	W
	0	0	0	0	0	0	0	0		
4F	eqqth[2:0]				eqcngsel[2:0]				05	W
	0	0	0	0	0	1	0	1		
50	cpet_off	cpe_off							00	W
	0	0	0	0	0	0	0	0		
51	cvcnth [7:0]								68	W
	0	1	1	0	1	0	0	0		
52	csioff	cvioff					fdoff	fdfm	20	W
	0	0	1	0	0	0	0	0		
54	ofsd[7:0]								57	W
	0	1	0	1	0	1	1	1		
55	scld[7:0]								F1	W
	1	1	1	1	0	0	0	1		
56	tvth[7:0]								20	W
	0	0	1	0	0	0	0	0		
57	fvth[7:0]								70	W
	0	1	1	1	0	0	0	0		
5C		cngsel[2:0]			cntdmax[3:0]				50	W
	0	1	0	1	0	0	0	0		
5D			cntumax[5:0]						00	W
	0	0	0	0	0	0	0	0		
5F	plroff								00	W
	0	0	0	0	0	0	0	0		
70	dintoff	dscroff	okval[2:0]			erval[2:0]			18	W
	0	0	0	1	1	0	0	0		
71	rsoff	revck	palonff	ipbval	msoff	laysel[2:0]			00	W
	0	0	0	0	0	0	0	0		
72				rmsk[2:0]					00	W
	0	0	0	0	0	0	0	0		
75		beron	rlocksw		nuckz		chclkp		00	W
	0	0	0	0	0	0	0	0		
76	auto_nul	cyc[2:0]			nuval	anuval	asyncng	perst	02	W
	0	0	0	0	0	0	1	0		
77	shsc[2:0]			shsl[2:0]			tsch	cor	00	W
	0	0	0	0	0	0	0	0		
7C						grgain[2:0]			00	W
	0	0	0	0	0	0	0	0		
7D		gripklv[2:0]				gropklv[2:0]			52	W
	0	1	0	1	0	0	1	0		
7F					gract	grovnum[2:0]			00	R
	0	0	0	0	0	0	0	0		
80	retryov	alarm	tmunvld	mdunvld	fulock	vulock	rulock	rseorf	00	R
	0	0	0	0	0	0	0	0		

81	emerg	tmcchg	cdunvld	slpen					00	R
	0	0	0	0	0	0	0	0		
82	ifagc_dt[7:0]								00	R
	0	0	0	0	0	0	0	0		
83	rfagc_dt[7:0]								00	R
	0	0	0	0	0	0	0	0		
84	carafc_dt[15:8]								00	R
	0	0	0	0	0	0	0	0		
85	carafc_dt[7:0]								00	R
	0	0	0	0	0	0	0	0		
86	clkafc_dt[15:8]								00	R
	0	0	0	0	0	0	0	0		
87	clkafc_dt[7:0]								00	R
	0	0	0	0	0	0	0	0		
89	mondati[7:0]								00	R
	0	0	0	0	0	0	0	0		
8A	mondatq[7:0]								00	R
	0	0	0	0	0	0	0	0		
8B	cndat[23:16]								00	R
	0	0	0	0	0	0	0	0		
8C	cndat[15:8]								00	R
	0	0	0	0	0	0	0	0		
8D	cndat[7:0]								00	R
	0	0	0	0	0	0	0	0		
8E	fvar[7:0]								00	R
	0	0	0	0	0	0	0	0		
8F	tvar[7:0]								00	R
	0	0	0	0	0	0	0	0		
90		eqqdt[2:0]			cvimax[11:8]				00	R
	0	0	0	0	0	0	0	0		
91	cvimax[7:0]								00	R
	0	0	0	0	0	0	0	0		
92				cviloc[12:8]					00	R
	0	0	0	0	0	0	0	0		
93	cviloc[7:0]								00	R
	0	0	0	0	0	0	0	0		
94	fddet				cvim[11:8]				00	R
	0	0	0	0	0	0	0	0		
95	cvim[7:0]								00	R
	0	0	0	0	0	0	0	0		
96	rlocka	rlockb	rlockc						00	R
	0	0	0	0	0	0	0	0		
97	verra[15:8]								00	R
	0	0	0	0	0	0	0	0		
98	verra[7:0]								00	R
	0	0	0	0	0	0	0	0		
99	verrb[15:8]								00	R
	0	0	0	0	0	0	0	0		
9A	verrb[7:0]								00	R
	0	0	0	0	0	0	0	0		
9B	verrc[15:8]								00	R
	0	0	0	0	0	0	0	0		
9C	verrc[7:0]								00	R
	0	0	0	0	0	0	0	0		
9D	perra[23:16]								00	R
	0	0	0	0	0	0	0	0		
9E	perra[15:8]								00	R
	0	0	0	0	0	0	0	0		

9F	perra[7:0]								00	R
	0	0	0	0	0	0	0	0		
A0	perrb[23:16]								00	R
	0	0	0	0	0	0	0	0		
A1	perrb[15:8]								00	R
	0	0	0	0	0	0	0	0		
A2	perrb[7:0]								00	R
	0	0	0	0	0	0	0	0		
A3	perrc[23:16]								00	R
	0	0	0	0	0	0	0	0		
A4	perrc[15:8]								00	R
	0	0	0	0	0	0	0	0		
A5	perrc[7:0]								00	R
	0	0	0	0	0	0	0	0		
A6	pecya[15:8]								00	R
	0	0	0	0	0	0	0	0		
A7	pecya[7:0]								00	R
	0	0	0	0	0	0	0	0		
A8	pecyb[15:8]								00	R
	0	0	0	0	0	0	0	0		
A9	pecyb[7:0]								00	R
	0	0	0	0	0	0	0	0		
AA	pecyc[15:8]								00	R
	0	0	0	0	0	0	0	0		
AB	pecyc[7:0]								00	R
	0	0	0	0	0	0	0	0		
AC				s_infom			agcim		00	R
	0	0	0	0	0	0	0	0		
AD	wunvld								00	R
	0	0	0	0	0	0	0	0		
B0	ffsize[1:0]		gdleng[1:0]		seqen[3:0]				A0	R/W
	1	0	1	0	0	0	0	0		
B1	woffset[7:0]								02	R/W
	0	0	0	0	0	0	1	0		
B2	sysid[1:0]		pachg[3:0]				emeflg	part	3D	R/W
	0	0	1	1	1	1	0	1		
B3	a_cnst[2:0]			a_rate[2:0]			a_ileav[2:1]		25	R/W
	0	0	1	0	0	1	0	1		
B4	a_ileav[0]	a_seg[3:0]			b_cnst[2:0]				8B	R/W
	1	0	0	0	1	0	1	1		
B5	b_rate[2:0]			b_ileav[2:0]			b_seg[3:2]		4B	R/W
	0	1	0	0	1	0	1	1		
B6	b_seg[1:0]		c_cnst[2:0]			c_rate[2:0]			3F	R/W
	0	0	1	1	1	1	1	1		
B7	c_ileav[2:0]			c_seg[3:0]				phcomp[2]	FF	R/W
	1	1	1	1	1	1	1	1		
B8	phcomp[1:0]		resva[5:0]						FF	R/W
	1	1	1	1	1	1	1	1		
B9	resvb[5:0]								FC	R/W
	1	1	1	1	1	1	0	0		
BA				monadr[12:8]					00	W
	0	0	0	0	0	0	0	0		
BB	monadr[7:0]								00	W
	0	0	0	0	0	0	0	0		
BC	sp_hold	monsel							00	W
	0	0	0	0	0	0	0	0		
C7		groff							00	W
	0	0	0	0	0	0	0	0		

C8				gr1dly[12:8]					00	R
	0	0	0	0	0	0	0	0		
C9	gr1dly[7:0]								00	R
	0	0	0	0	0	0	0	0		
CA				gr2dly[12:8]					00	R
	0	0	0	0	0	0	0	0		
CB	gr2dly[7:0]								00	R
				0	0	0	0	0		
CC				gr3dly[12:8]					00	R
	0	0	0	0	0	0	0	0		
CD	gr3dly[7:0]								00	R
	0	0	0	0	0	0	0	0		
DA	dagc_dt[7:0]								00	R
	0	0	0	0	0	0	0	0		
E4	schnum[3:0]				initnum[3:0]				84	W
	1	0	0	0	0	1	0	0		
EC					recvmdsel				00	W
	0	0	0	0	0	0	0	0		
EF							sydfmd[1:0]		00	W
	0	0	0	0	0	0	0	0		
FE	tnflg[7:0]								00	W
	0	0	0	0	0	0	0	0		

* The shaded areas indicate unused or test registers. Do not set a value different from the initial value.
* For some registers, a value that differs from the initial value must be set during normal operation as well. (Refer to the evaluation software.)
* Under R/W, "W" indicates a write-only register and "R" indicates a read-only register. Note that the value written in the "W" register can be checked by reading the value from the same register address, excluding the following registers:

Address 01h	Data [7]	isyrst
	Data [6]	imsrst
	Data [4]	iwsrst
Address 76h	Data [0]	perst
Address FEh	Data [7:0]	tnflg[7:0]

* The registers with XSEL described in their "Initial value" column are set automatically when some or all of them are reset to SYRSTN by the XSEL1 and XSEL0 pins. Bits that are set automatically are indicated by "-".

6. I/O Interface

6.1 PSK Demodulation IF Input Interface

The TC90512XBG PSK demodulator uses the orthogonal detected IQ baseband signals as input. The input PSK signals are AD converted inside the IC and subjected to demodulation and error-correction processing. The following describes the IQ signal interface:

1) Input format: IQ baseband format, differential/single-ended input
- Since a bias circuit is contained, no external bias resistors are required. IF signals are input directly after DC decoupling.
- In the case of single-ended input, connect the input to AIP that is AC grounded to the AIN.

2) Input impedance: 10 kΩ// (reference value:7pF)

3) ADC dynamic range: Differential voltage 0.75 Vp-p (changeable in the range of 0.5 to 1.5 Vp-p by adfs)

4) Rated input level: Differential voltage 0.375Vp-p typ. (In terms of sine wave, 1/2 of the dynamic range. Adaptively controlled in accordance with input C/N.)

5) IQ orthogonal deviation correction range: ±5° typ.

6) IQ gain deviation correction range: ±2 dB typ.

7) Carrier pull-in range: ±5 MHz typ.

8) Clock allowable frequency deviation: ±200 ppm typ.

6.2 OFDM Demodulation IF Input Interface

The TC90512XBG OFDM demodulator uses the OFDM signals converted to IF (intermediate frequency) or the orthogonal detected IQ baseband signals as input. The input OFDM signals are AD converted inside the IC and subjected to I/Q detection, demodulation, and error-correction processing. The following describes the IF signal interface:

1) Input format: IF or IQ baseband format, differential/single-ended input
- Since a bias circuit is contained, no external bias resistors are required. IF signals are input directly after DC decoupling.
- In the case of single-ended input, connect the input to AIP that is AC grounded to the AIN.

2) Input impedance: 10kΩ // (reference value: 7pF)

3) ADC dynamic range: Differential voltage 1 Vp-p

4) Rated input level: Differential voltage 290 mVp-p typ. (sine wave converted, tentative value)

5) IF center frequency: 4 MHz, 44 MHz, 57 MHz

6) Carrier allowable frequency deviation: ±250 kHz typ. (13-segment reception mode)
±200 kHz typ. (1- or 3-segment reception mode)

7) Clock allowable frequency deviation: ±200 ppm typ.

8) Correction range for the IQ baseband input signals: gain deviation ±1.5 dB typ and orthogonal deviation ±5° typ.

[Important] The clock allowable frequency deviation is the frequency deviation related to variance, aging and long-term drift. It does not include short-term sudden frequency changes such as at power ON.
Specifically, when discontinuity exists in crystal frequency - temperature characteristics and a sudden frequency change occurs at a relatively small temperature change, demodulation S/N deterioration and a demodulation error may result. Caution is required.

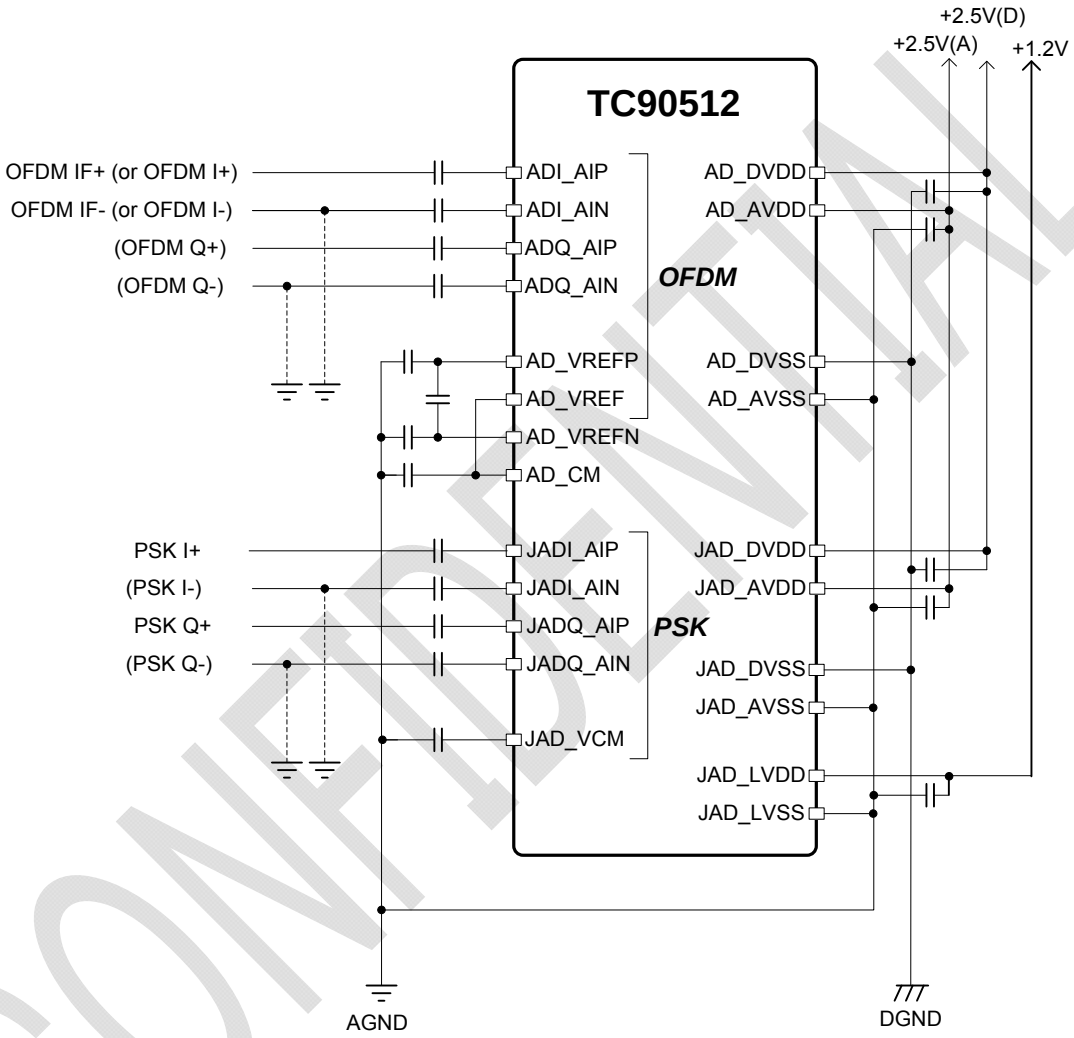


Fig. 6.1 Analog Input Interface

* Both OFDM input and PSK input do not require external bias voltage supply since DC bias voltage is applied in IC internal circuitry.
* For OFDM, IQ baseband signals can be input in addition to IF input. In this case, selection is possible between single-ended input and differential input.
* In the case of single-ended input, the input is grounded to the analog GND as shown by the dashed lines in the figure. (To reduce the effect of noises, use of differential input is recommended.)

OFDM register map

Name	Address (HEX)	Data	R/W	Initial Value	Description
adfs	85	[5:4]	W	0x1	Select an ADC full-scale differential voltage for PSK. 0: 0.5 Vp-p 1: 0.75 Vp-p 2: 1.0 Vp-p 3: 1.5Vp-p

6.3 TS Output Interface

TC90512XBG outputs TS in parallel or serial format. TS outputs for PSK demodulation and OFDM demodulation are independently provided.

[Important] The byte clock of this IC is generated by dividing the burst clock that decimated the reference clock. In consequence, the TS serial clock duty ratio is not constant. In addition, the clock frequency in OFDM narrow-band reception mode is the same as that in wide-band reception mode.

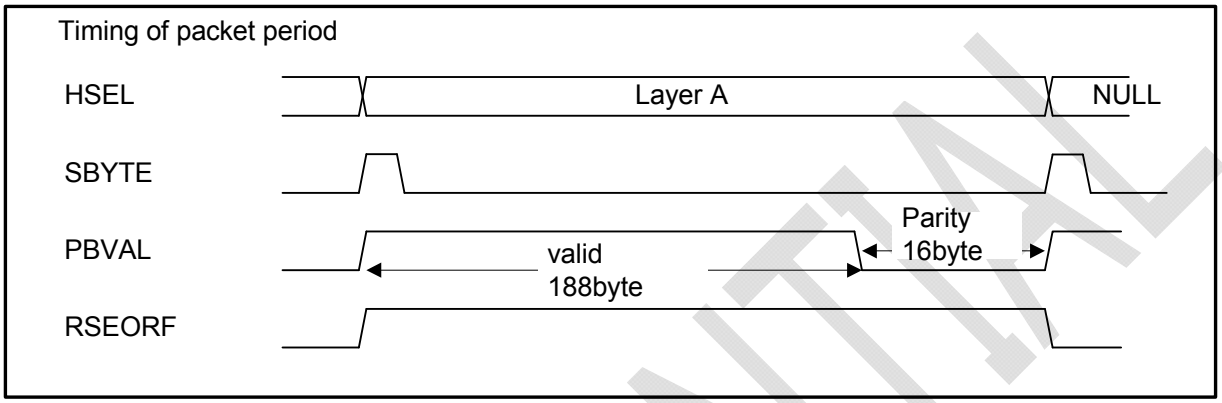


Fig. 6.3 TS Output Format (Packet Cycle)

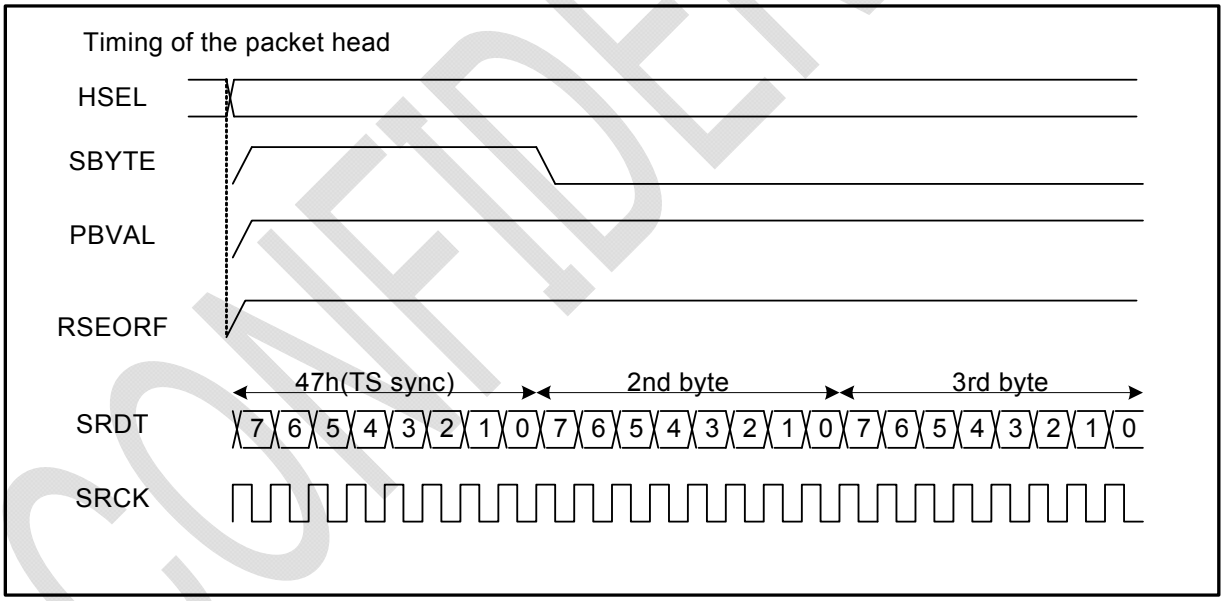


Fig. 6.4 Serial TS Output Format

HSEL: Valid/Null packet ID flag
SBYTE: Packet synchronization
PBVAL: Information byte period flag
RSEORF: Packet error flag
SRDT: TS serial data (including parity bits)
SRCK: TS serial clock

* **PSK pins have "J" attached to the above signal names**.

6.4 Clock Input

TC90512 supports two clock modes for clock generation: "XO mode" which is based on a crystal oscillator (XO), and "external clock mode" which inputs clock data from an external source.
The IC built-in PLL is synchronized with the master clock required for OFDM demodulation and PSK demodulation and is generated using crystal oscillation output or the external clock as standard.

6.4.1 XO Mode (with Crystal Directly Mounted)

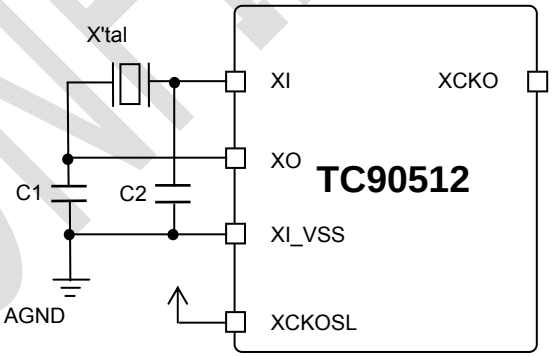
The crystal frequencies that can be used in XO mode (with crystal directly mounted) are shown below. The applicable crystal frequency range differs according to the OFDM input IF frequency.

(1) When OFDM input is 57 MHz IF: The crystal frequency is 25.400 MHz
The IC can operate on other frequencies if register settings are changed.
For details, refer to Section 6.5.

(2) When OFDM input is 4 MHz IF: The crystal frequency is 4.000 MHz.
The IC can operate on other frequencies if register settings are changed.
For details, refer to Section 6.5.

(3) When OFDM input is IQ baseband: The crystal frequency is 4.000 MHz.
The IC can operate on other frequencies if register settings are changed.
For details, refer to Section 6.5.

The settings of the clock division ratio differ with the crystal frequencies. The settings are made by the XSEL1 and XSEL0 pins and the iexdiv and ilpdiv registers. The initial values of the iexdiv and ilpdiv registers are set by the XSEL1 and XSEL0 pins, captured into the IC when the power-on reset (system reset) is "0," and confirmed when it changes from "0" to "1."
For a setting example of the clock division ratio at each crystal frequency and clock frequency selection precautions, refer to Section 6.5.



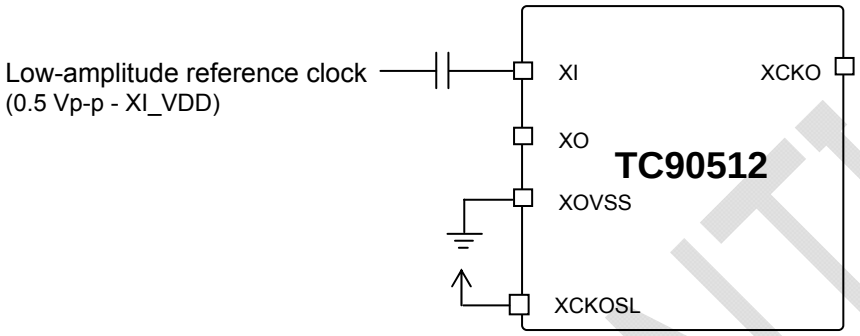
C1=10pF (reference value)
C2=10pF (reference value)

* The optimum values for the capacitors C1 and C2 differ according to the crystal to be used. If they are not set properly, deviation of the oscillation frequency and degradation of the negative resistance may be caused.
* To prevent XCKO spurious interferences, stop the output by XCKOSL or by setting the ixckosl register to "1."

Fig. 6.4 XO (with Crystal Directly Mounted) Mode

6.4.2 External Clock Mode

The external clock mode generates the master clock from the low amplitude (0.5 Vp-p to XOVDD) clock signal input from the XI pin. The applicable external reference clock frequency is the same as for the XO mode (crystal directly mounted). The method of setting the clock division ratio is also the same.
Low-amplitude clocks are supplied to XI pin through AC coupling. When default values are used, inverted clocks and noninverted clocks are output to the XO and XCKO pins, respectively. This output can be stopped by setting each of the ixosl and ixckosl registers to "1."
Note that the XI pin is used as a 2.5 V I/O power supply. Do not enter clocks with an amplitude (p-p) more than the 2.5 V (XI_VDD) power supply voltage. The XO and XCKO pins are also used as 2.5 V I/O power supply.



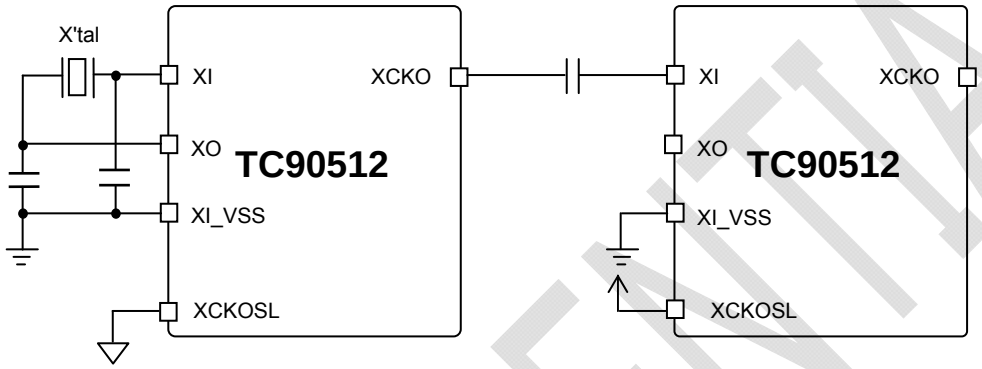
* Signals of the VDDS (3.3 V) level cannot be input to the XI pin.
* To prevent spurious interferences, the clock output of the XO and XCKO pins must have been stopped by XCKOSL or by setting the ixckosl register to "1."

Fig. 6.5 External Clock Mode (Low-Amplitude Reference Clock Input)

6.4.3 Clock Distribution Mode

TC90512 is provided with an output pin for distributing the reference clock to other ICs. If multiple TC90512s are used, for example, the reference clock can be distributed to them from only one crystal. Note that, when multiple TC90512s are used, a different I^2C slave address must have been set for each of TC90512s.

[Important] The number of ICs to which the reference clock can be distributed differs with the load and noises. Clock distribution to the maximum number of slave addresses is not guaranteed.



* The IC to which the crystal is connected must be set with ixosl="0" and ixckosl="0" (default settings).
* As for the ICs to which the crystal is not connected, to prevent spurious interferences, the clock output of the XO and XCKO pins must have been stopped by setting ixosl = "1" or XCKOSL (or ixckosl) = "1."

Fig. 6.6 Distribution of the Reference Clock

OFDM register map

Name	Address (HEX)	Data	R/W	Initial Value	Description
ixckosl	04	[1]	W	XCKOSL	Stop the output of the distribution output XCKO. 0: XCKO output ON 1: XCKO output OFF
ixosl	04	[0]	W	0x0	Stop the XO output. 0: XO output ON 1: XO output OFF

6.5 Setting the IF Frequency and Clock Frequency

Table 6-1 shows default values to specify the OFDM input signal frequency and the reference clock (crystal) frequency XT of TC90512. The clock-related registers are set automatically by setting the XSEL1 and XSEL0 pins. For setting examples of the frequency-related registers, refer to Chapter 10. For settings for frequencies not listed in the Table, refer to the next paragraph and after. (The center frequency of TC90512 OFDM IF can be set to a value other than 57 MHz. For example, 44 MHz can be set. However, this requires settings of individual registers, so contact Toshiba for more information.)

Table 6-1 Reference Clock Frequency, MD, and Serial Clock Relationship

Clock Operation Mode	XSEL1 pin	XSEL0 pin	IF center frequency of OFDM [MHz]	Reference Clock Frequency XT [MHz]	Master clock Frequency MD(Note) [MHz]	OFDM serial TS clock Frequency [MHz]	PSK serial TS clock Frequency [MHz]
57 MHz IF (XT=25 MHz)	0	0	57.000	25.400	76.200 (3XT)	38.100	60.960
57 MHz IF (XT=20 MHz)	0	1	57.000	20.500	82.000 (4XT)	41.000	65.600
4 MHz IF (XT=4 MHz)	1	0	4.063	4.000	78.000	39.000	62.400
4 MHz IF (XT=27 MHz)	0	0	4.063	27.000	81.000	40.500	64.800
IQ baseband (XT=4 MHz)	1	1	0.000	4.000	78.000	39.000	62.400

Note) The lower limit value of MD is 76.157 MHz. Normal operation is not possible if a value lower than this limit value is set.

Figure 6.7 shows a block diagram of the clock generation PLL. The iexdiv register is set with a clock division ratio of 1/m for the reference clock and the ilpdiv register is set with a clock generation ratio of 1/n for the VCO (voltage control oscillator). The XSEL1 and XSEL0 pins are used to set the initial values of these registers.
The AD sampling frequency is XT for the 57 MHz IF (direct IF) mode of OFDM. It is MD/4 for the 4 MHz (low IF) mode. The TS serial clock of OFDM has a frequency obtained by dividing MD by 2. The TS serial clock of PSK has a frequency obtained by multiplying MD by 4/5. Each TS parallel clock (byte clock) has a frequency of one-eighth the respective TS serial clock.
In any clock operation mode, however, **normal operation is impossible** if the master clock MD is less than 76.157 MHz. **Make sure that the master clock MD is always above the lower limit value with consideration to the center frequency deviation, temperature change, and age deterioration of the crystal**.

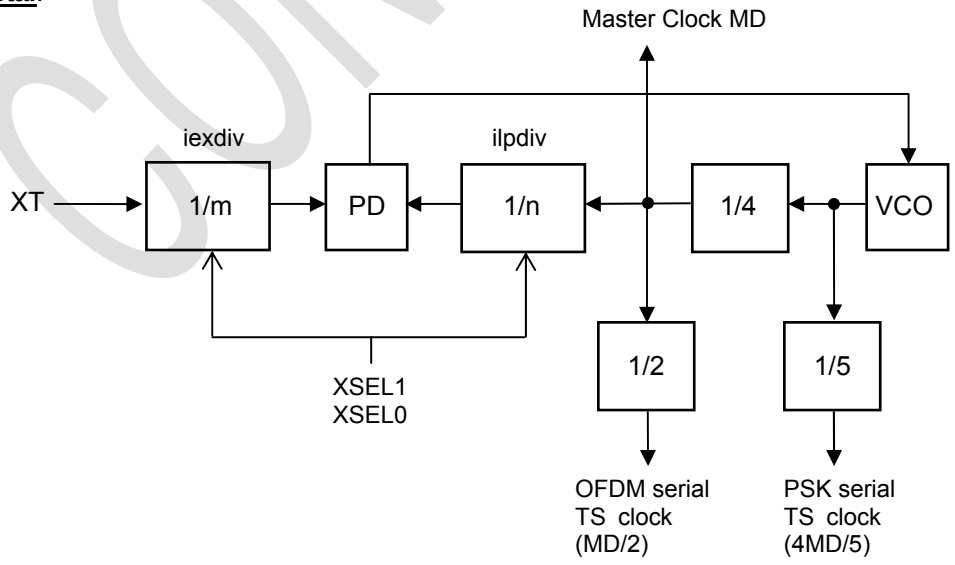


Fig. 6.7 Block Diagram of the Clock Generation PLL

6.5.1 Setting the 57 MHz IF (XT=25 MHz) Mode

In 57 MHz IF (XT=25 MHz) mode, 57 MHz IF is under sampled by a frequency of 2XT. This mode is effective when the vertical adjacent channels do not wrap around within the band but relatively more out-of-band components remain in the input IF signal. When both the XSEL1 and XSEL0 registers are set to "0," the following registers are set automatically in accordance with the reference clock frequency XT set to 25.400 MHz.

- iexdiv= "0Bh" (11) : PLL division ratio (reference clock side)
- ilpdiv= "21h" (33) : PLL division ratio (VCO side)
- hkfrq= "2C0Ah" (11,274) : OFDM clock frequency offset correction
- cpld_dt= "0FA0h" (4,000) : OFDM carrier frequency offset correction
- affrq= "170h" (368) : Carrier AFC loop gain correction
- lpfsl= "3h" : OFDM digital filter
- f_inv= "1" : OFDM frequency polarity
- jhkfrq= "51F6h" (20,982) : PSK clock frequency offset correction
- afcg= "52h" (82) : PSK carrier AFC loop gain correction

When you change the reference clock frequency XT of 25.400 MHz, select an XT value in the range of XT=25.386 to 26.111 MHz. (Normal operation is possible only when the XT value is within this range.) The lower the XT frequency is, the less the folding of the upper adjacent channel is, while on the other hand, the folding of the lower adjacent channel is more liable to get into the bandwidth. On the other hand, the higher the XT frequency is, the less the folding of the lower adjacent channel is, while the folding of the upper adjacent channel is liable to get into the bandwidth.
Note that the set value of the hkfrq, cpld_dt, affrq, jhkfrq, and afcg registers must be changed when the XT frequency is changed.

6.5.2 Setting the 57MHz IF (XT=20MHz) Mode

In 57 MHz IF (XT=20 MHz) mode, 57 MHz IF is under sampled by a frequency of 3XT. Since the AD sampling frequency becomes lower and the vertical adjacent channels wrap around within the band, it is required to suppress out-of-band components of the input IF signal adequately. When the XSEL1 pin is set to "0" and the XSEL0 pin is set to "1," the following registers are set automatically in accordance with the reference clock frequency XT set to 20.500 MHz.

- iexdiv= "08h" (8) : PLL division ratio (reference clock side)
- ilpdiv= "20h" (32) : PLL division ratio (VCO side)
- hkfrq= "42E0h" (17,120) : OFDM clock frequency offset correction
- cpld_dt= "0E0Dh" (3,597) : OFDM carrier frequency offset correction
- affrq= "0D4h" (212) : Carrier AFC loop gain correction
- lpfsl= "2h" : OFDM digital filter
- f_inv= "0" : OFDM frequency polarity
- jhkfrq= "6BB0h" (27,568) : PSK clock frequency offset correction
- afcg= "4Ch" (76) : PSK carrier AFC loop gain correction

When you change the reference clock frequency XT of 20.500 MHz, select an XT value in the range of XT=20.467 to 20.750 MHz. When the XT frequency is changed, the set value of the hkfrq, cpld_dt, affrq, jhkfrq, and afcg registers must be changed.

6.5.3 Setting the 4 MHz IF (XT=4 MHz) Mode

In 4MHz IF mode, 4 MHz IF is sampled by a frequency of MD/4. When the XSEL1 pin is set to "1" and the XSEL0 pin is set to "0," the following registers are set automatically in accordance with the reference clock frequency XT set to 4.000 MHz.

- iexdiv= "02h" (2) : PLL division ratio (reference clock side)
- ilpdiv= "27h" (39) : PLL division ratio (VCO side)
- hkfrq= "3320h" (13,088) : OFDM clock frequency offset correction

- cpld_dt= "0D56h" (3,414) : OFDM carrier frequency offset correction
- affrq= "0AAh" (170) : OFDM carrier AFC loop gain correction
- lpfsl= "0h" : OFDM digital filter
- f_inv= "0" : OFDM frequency polarity
- jhkfrq= "59F2h" (23,026) : PSK clock frequency offset correction
- afcg= "50h" (80) : PSK carrier AFC loop gain correction

6.5.4 Setting the 4 MHz IF (XT=27 MHz) Mode

When the 4 MHz IF is used on the reference clock frequency XT=27.000 MHz, set both the XSEL1 and XSEL0 pins to "0," and then set the following registers. The sampling frequency is MD/4.

- hkfrq= "3EF0h" (16,112) : OFDM clock frequency offset correction
- cpld_dt= "0CD8h" (3,288) : OFDM carrier frequency offset correction
- affrq= "0CAh" (202) : OFDM carrier AFC loop gain correction
- lpfsl= "0h" : OFDM digital filter
- f_inv= "0" : OFDM frequency polarity
- jhkfrq= "6740h" (26,432) : PSK clock frequency offset correction
- afcg= "4Dh" (77) : PSK carrier AFC loop gain correction

Note that the following registers are set automatically when both the XSEL1 and XSEL0 pins are set to "0."

- iexdiv= "0Bh" (11) : PLL division ratio (reference clock side)
- ilpdiv= "21h" (33) : PLL division ratio (VCO side)

6.5.5 Setting the IQ Baseband (XT=4 MHz) Mode

In IQ baseband mode, the IQ baseband signal is sampled by a frequency of MD/4. When the XSEL1 pin is set to "1" and the XSEL0 pin is set to "0," the following registers are set automatically in accordance with the reference clock frequency XT set to 4.000 MHz.

- iexdiv= "02h" (2) : PLL division ratio (reference clock side)
- ilpdiv= "27h" (39) : PLL division ratio (VCO side)
- hkfrq= "3320h" (13,088) : OFDM clock frequency offset correction
- cpld_dt= "0000h" (0) : OFDM carrier frequency offset correction
- affrq= "0AAh" (170) : OFDM carrier AFC loop gain correction
- lpfsl= "0h" : OFDM digital filter
- f_inv= "0" : OFDM frequency polarity
- jhkfrq= "59F2h" (23,026) : PSK clock frequency offset correction
- afcg= "50h" (80) : PSK carrier AFC loop gain correction

OFDM register map

Name	Address (HEX)	Data	R/W	Initial Value	Description
ilpdiv [5:0]	11	[5:0]	W	XSEL	Clock division ratio (PLL side) setting Clock division ratio n=1 to 63
iexdiv [4:0]	12	[4:0]	W	XSEL	Clock division ratio (external side) setting Clock division ratio m=1 to 31

* The initial value XSEL is determined by the settings of the XSEL1 and XSEL0 pins.

* The set value of the hkfrq, cpld_dt, affrq, jhkfrq, and afcg registers must be changed. For detail, see Sections 8.4, 8.6, 9.5, and 9.8.

6.6 AGC Output

AGC output generates a DC control signal based on the change of density of the pulse. The pulse amplitude is nearly from GND to the I/O power supply voltage, so that if the entire pulse amplitude is "H," VDDS DC voltages are generated and if the entire pulse amplitude is "L," voltages close to the GND potential are provided.
As the OFDM AGC output, RF_AGC and IF_AGC are independently provided. Use as IF single AGC control, however, is also possible.
The output H level is 3.3 V and cannot be pulled up to 5 V.

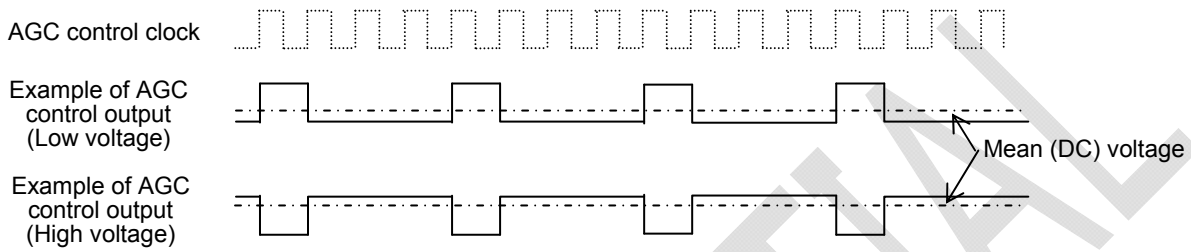


Fig. 6.8 AGC Output Waveform

The AGC output format is "H" and "L" diffused 1-bit DAC format, as shown in Figure 6.9. Since the harmonic components of PWM control frequency are diffused to high frequency, suppression using an external LPF filter is easy.

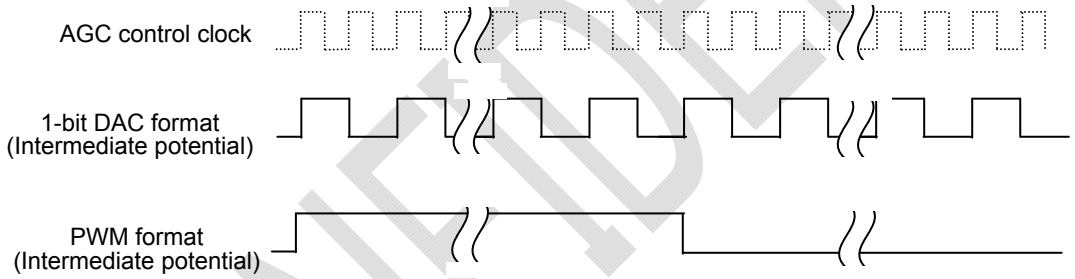


Fig. 6.9 AGC Output Waveform in 1-bit DAC Format

AGC output is digital output but is treated as analog output when supplied to the tuner AGC control input pin, so care should be taken to prevent noises from being mixed. Inserting resistance of 10 to 20 kΩ in series near the AGC output pin is sometimes effective in reducing spurious characteristics. This resistance can be regarded as part of the LPF filter.

6.7 Output Control

TC90512 designated output pins are grouped into System A, System B, System C and System D pins, as indicated below, allowing you to set each of the output signal systems.

Table 6-2 Output Controllable Pin Systems

Pin System	Pin Number									
	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
System A pins	H15	H14	D15	D14	E15	E14	F15	F12	G15	G14
System B pins	A9	B9	A10	B10	A11	B11	A12	B12	A13	B13
System C pins	A4	B4	A5	B5	A6	B6	A7	B7	A8	B8
System D pins	G1	G2	C1	C2	D1	D2	E1	E2	F1	F2

The signal systems that can be set are described below.

Table 6-3 Output Controllable Signal Systems

Signal System	Signal Name									
	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
OFDM parallel	RLOCK	RERR	RSOUT 7	RSOUT 6	RSOUT 5	RSOUT 4	RSOUT 3	RSOUT 2	RSOUT 1	RSOUT 0
OFDM serial	SRCK	SRDT	RSCKO	SBYTE	PBVAL	RSEORF	STSFLG 1	STSFLG 0	FLOCK	SLPEN
PSK serial	JSRCK	JSRDT	JRSCKO	JSBYTE	JPBVAL	JRSEORF	JSTSFLG 1	JSTSFLG 0	JLOCK	JPORT
PSK parallel	JRLOCK H	JRLOCK L	JRSOUT 7	JRSOUT 6	JRSOUT 5	JRSOUT 4	JRSOUT 3	JRSOUT 2	JRSOUT 1	JRSOUT 0

By default, the following pin assignments are made:

System A pins: OFDM parallel (TS) signal
System B pins: OFDM serial (TS) signal
System C pins: PSK serial (TS) signal
System D pins: PSK parallel (TS) signal

By setting the specified registers, these assignments can be changed. For more information about registers, refer to Sections 8.3 and 9.4.

In addition, the registers (addresses 1Ch, 1Dh, 1Eh and 1Fh) of PSK and OFDM allow you to switch the initial state of PSK signal system and OFDM signal system to output enabled/disabled ("High-Z" or pull-down, depending on the pin). The initial state is output enabled when JOEN and OEN are "0" and output disabled when JOEN and OEN are "1." The JOEN and OEN pin settings are captured into the IC when the SYRSTN pin is "0" and confirmed when the SYRSTN pin changes from "0" to "1." (The OEN setting is also captured when the isyrst register is set, and the JOEN setting is also captured likewise.)

* OEN and JOEN are not used for output control for each pin system but they are used to provide the initial value for each signal system. To be specific, the setting of the OEN pin is not for the output control of Systems A and B, but it is the initial value of the output enable/disable control for the OFDM parallel and OFDM serial signal systems. Even after the pin assignment for these signal systems is changed, the output enable/disable setting initially set by OEN interlocks with the OFDM signal system. Similarly, the output enable/disable setting initially set by JOEN also interlocks with the PSK signal system.

Although the initial output state of each signal system immediately after power-on reset is set by the above-described OEN and JOEN pins, each state can be set to enabled/"High-Z" or pull-down/fixed to "0,"/fixed to "1" by setting the output enabled register corresponding to the signal. For more information about registers, refer to Sections 8.3 and 9.4.

OFDM register map

Name	Address (HEX)	Data	R/W	Initial Value	Description
pinsld [1:0]	0F	[7:6]	W	0x3	System D pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal
pinslc [1:0]	0F	[5:4]	W	0x3	System C pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal
pinslb [1:0]	0F	[3:2]	W	0x1	System B pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal
pinsla [1:0]	0F	[1:0]	W	0x0	System A pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal

7. Power-On Reset

TC90512 requires reset signal (SYRSTN) input for clock frequency dividing and register initialization at power ON. The settings of the XSEL1, XSEL0, SLADRS1, SLADRS0, OEN, and JOEN pins are captured into the IC when the SYRSTN pin is "0" and confirmed when the SYRSTN pin changes from "0" to "1."
Power-on reset is set to "1" after the IC is powered on with the SYRSTN pin set to "0" and the built-in PLL clock oscillation has stabilized. A "0" period of at least 10 ms after all power supplies have reached the specified minimum voltage value or higher is required for PLL stabilization and I^2C circuit initialization.
Start I^2C communication at least 1us after the reset signal has reached the specified "1" level.
Perform on/off operation of two or more power supplies of TC90512 simultaneously, or within a period of 100 ms. The sequence is not defined.

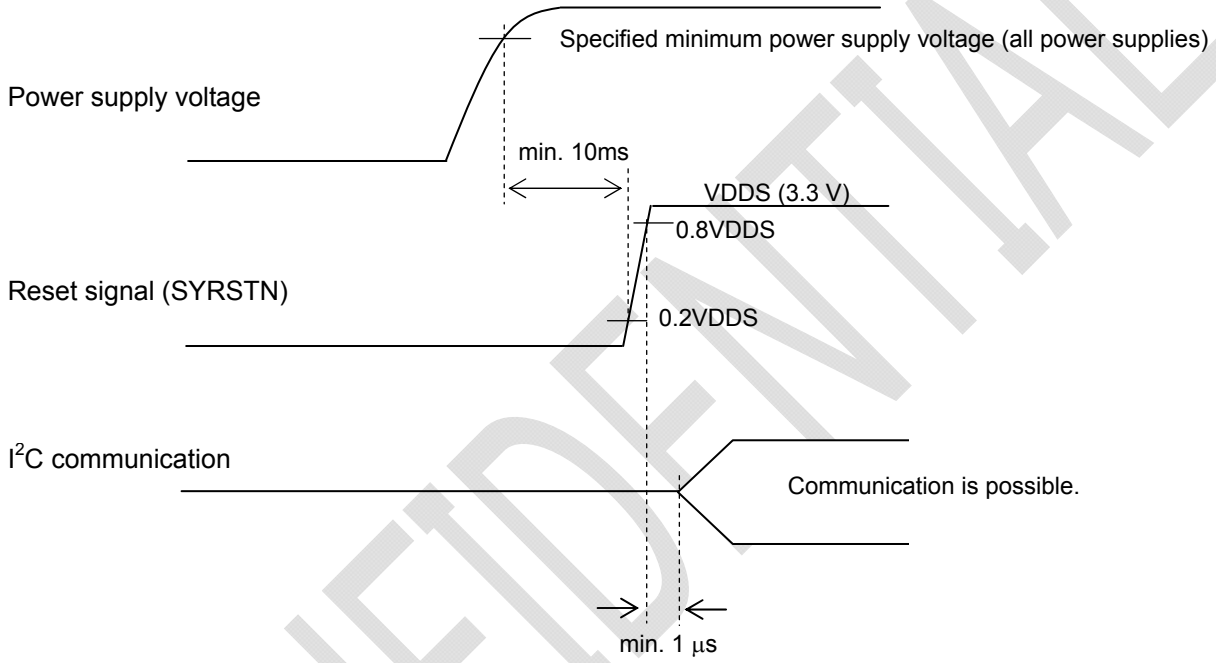


Fig. 7.1 Timing of Power-On Reset

Resetting the isyrst register initializes the total system including I^2C. About 4us after reset by isyrst=1, the setting automatically returns to "0." Thus, clearing isyrst to "0" afterward is not needed to stop the reset process. Note that, however, place I^2C in the stop status (issue the stop condition) to await the total initialization of the circuit before starting the next communication.
The pin status and the internal status before resetting cannot be defined. In some cases, much current dissipation may be involved since the clock PLL generation frequency is not defined. Therefore, be sure to perform power on resetting with the specified timing at the time of power on.

[Important] Perform on/off operation of two or more power supplies of simultaneously, and perform power-on reset at power on.

8. Digital Satellite (PSK) Demodulation Functions

8.1 Reset

The TC90512 OFDM demodulation circuit has the following two reset signals:
1) PSK system reset to initialize the entire PSK system (psksyrst)
2) PSK demodulation reset to initialize the demodulation synchronization sequence (pskmsrst)

Initialize all registers of the PSK demodulating part with psksyrst= "1." (In addition to power on resetting SYRSTN at the time of power on, psksyrst= "1" is also required.)Perform register setting 1 us after power on resetting described above or later. Set psksyrst= "1" before setting other PSK registers.

[Important] Be sure to set psksyrst= "1" before setting the registers in the PSK part.

After the above system reset and register initialization were performed, only PSK demodulation reset pskmsrst should be performed at the time of sub-channel tuning, thus eliminating the need for setting other registers.

Since these reset values automatically return to "0" about 4 us after their setting, there is no need for setting "0" to stop the reset process. As for I^2C communication, the reset process completes before the next communication begins, so any wait time is not needed in particular.

[Important] After power ON, **the PSK demodulation function is operating in its initial state**. Use the PSK demodulation standby function when power consumption needs to be reduced by stopping BS reception. (Refer to Section 8.2.)

Name	Address (HEX)	Data	R/W	Initial Value	Description
psksyrst	01	[7]	W	0x0	PSK system reset Initialize all the registers of the PSK demodulator. 0: Do not reset. 1: Reset.
pskmsrst	03	[0]	W	0x0	PSK demodulation reset Initialize the PSK demodulation synchronization circuit. 0: Do not reset. 1: Reset.

8.2 Standby Function

This function is used to stop (sleep status) the clock supply to the PSK demodulation circuit except its I^2C control to reduce power consumption. This IC, however, can also monitor the emergency alarm broadcasting start control signal transmitted by TMCC, while reducing power consumption, by performing modulation action (wakeup status) intermittently. The standby function can select any of the following three modes:

(1) Constant sleep status to reduce power consumption.
(2) Intermittent wakeup for monitoring the emergency alarm broadcasting start control signal
(3) Intermittent wakeup for monitoring the emergency alarm broadcasting start control signal, plus automatic resetting of sleep status while the start control signal is detected.

In any case, the AD conversion circuit assumes the sleep status with power down when register jslpadc="1," for lower power consumption

8.2.1 Continuous Sleep

To select the first mode, set any value other than "0" in the sleep period set register watim and set "0" in the wakeup period set register tetim.

8.2.2 Monitoring the Startup Control Signal (without Startup Control)

To select the second mode, set jslpmd ="0" and any value other than "0" in both of watim and tetim. Then the sleep status alternates with the wakeup status even when the start control signal is detected. The start control signal can be monitored in register emgcy and is output in the JSTSFLG0 pin. (For details, see Section 8.3.4.)

Table 8.1 Setting the PSK Demodulation Standby Operation (without Startup Control)

jslpmd ="0"		Wakeup time	
		tetim="0"	tetim ≠ "0"
Sleep time	watim="0"	Continuous wakeup	Continuous wakeup
	watim ≠ "0"	Continuous sleep	Sleep and wakeup are repeated alternately.

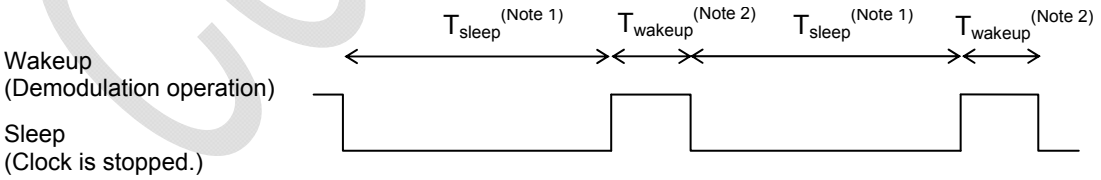


Fig. 8.1 Standby Operation without Startup Control

Note 1) Sleep period T_{sleep} is obtained by watim setting x 0.58 + 0.3 [s]. For sleep, watim can be set in the range of 1 to 255 and the sleep time is $0.9s \leq T_{sleep} \leq 148s$.

Note 2) Wakeup time T_{wakeup} is obtained by tetim setting x 0.58 + 0.3 [s]. For wakeup, tetim can be set in the range of 1 to 31 and the wait time is $0.9s \leq T_{wakeup} \leq 18s$.

8.2.3 Monitoring the Startup Control Signal (with Startup Control)

To select the third mode, set jslpmd="1" and any value other than "0" in both of watim and tetim. The wakeup status continues as long as the emergency alarm broadcasting start control signal is detected, and the sleep status alternates with the wakeup status while that signal is not detected. The use of the sleep period set register and the wakeup period set register including the method of their setting are the same as those for a case where start control is not performed.
It is possible to make modulation operation occur on detection of the start control signal only when each layer of the selected TS is judged free of error (rlockl="1" or rlockh="1"), by setting the emgmsk register to "1." For more information about error judgment, refer to Section 8.9.9.

Table 8.2 Setting the PSK Demodulation Standby Operation (with Startup Control)

jslpmd="1"		Wakeup time	
		tetim="0"	tetim ≠ "0"
Sleep time	watim="0"	Continuous wakeup	Continuous wakeup
	watim ≠ "0"	Continuous sleep	Sleep and wakeup are repeated alternately and wakeup is continued in the startup control signal detection period.

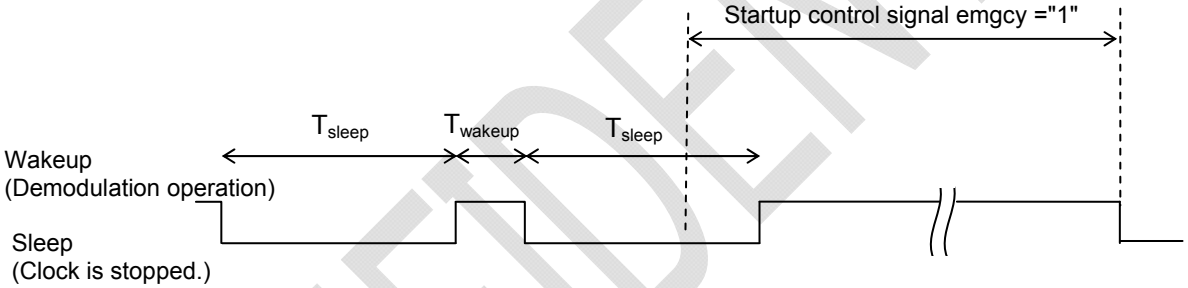


Fig. 8.2 Standby Operation with Startup Control

8.2.4 LNB Power Supply Control

The LNB (Low Noise Block-down-converter) power supply control signal can be output to the JPORT pin that interlocks with the standby operation by setting the atpt register to "1." The LNB power supply control signal assumes "0" in the sleep status and "1" in the wakeup status.

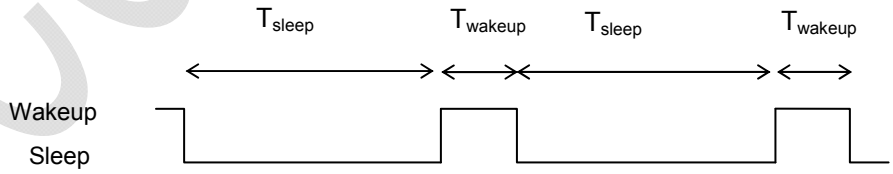


Fig. 8.3 Linkage of LNB Power Supply Control

Name	Address (HEX)	Data	R/W	Initial Value	Description
emgmsk	04	[4]	W	0x0	Set the wakeup conditions with startup control provided. 0: Always return to demodulation operation when the startup control signal is detected (emgcy="1"). 1: Return to demodulation only when the selected TS contains no error (rlockl="1" or rlockh="1") on startup control signal detection (emgcy="1"). * The JSTSFLG0 pin is linked to the operation described above.
jslpadc	13	[7]	W	0x0	Set ADC power down. 0: Do not power down the ADC for sleep. 1: Power down the ADC for sleep.
atpt	13	[6]	W	0x0	Set the LNB power supply control (JPORT output links to wakeup). (The bpot_en setting has a high priority.) 0: Output the jport setting (0: Low, 1: High-Z). 1: "0" in the Tsleep period, "1" in other periods
jslpmd	13	[5]	W	0x0	Set the operation when the startup control signal is detected. 0: Do not return to the demodulation operation when the startup control signal emgcy="1." 1: Return to the demodulation operation when the startup control signal emgcy="1."
tetim [4:0]	15	[4:0]	W	0x00	Set the wakeup time. This time can be set in steps of about 0.6 seconds. 0: Do not demodulate. (Modulate when watim="0.") 1 to 31: Wakeup time T_{wakeup}=tetim setting x 0.58 + 0.3 [s] ($0.9s \leq T_{wakeup} \leq 18s$)
watim [7:0]	17	[7:0]	W	0x00	Set the sleep time. This time can be set in steps of about 0.6 seconds. 0: Always demodulate. 1 to 31: Sleep time T_{sleep}=watim setting x 0.58 + 0.3 [s] ($0.9s \leq T_{sleep} \leq 148s$)

8.3 Input/Output Settings

8.3.1 Input Settings

ADC is either a differential or single-ended input. Since a bias resistor is contained, signals are input via AC coupling. In the case of single-ended input, AC-ground the pins that are not used to the analog GND. The iqch register allows you to switch the I and Q signals.

8.3.2 Output Pin Switching

Designated output pins are grouped into System A, System B, System C and System D pins, as indicated below, allowing you to assign output signals each system. (Refer to Section 6.7.)

Pin System	Pin Number									
	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
System A pins	H15	H14	D15	D14	E15	E14	F15	F12	G15	G14
System B pins	A9	B9	A10	B10	A11	B11	A12	B12	A13	B13
System C pins	A4	B4	A5	B5	A6	B6	A7	B7	A8	B8
System D pins	G1	G2	C1	C2	D1	D2	E1	E2	F1	F2

Signal System	Signal Name	Function
PSK (Parallel TS)	JRLOCKH	High-layer error free flag
	JRLOCKL	Low-layer error free flag
	JRSOUT7	TS parallel data 7 output
	JRSOUT6	TS parallel data 6 output
	JRSOUT5	TS parallel data 5 output
	JRSOUT4	TS parallel data 4 output
	JRSOUT3	TS parallel data 3 output
	JRSOUT2	TS parallel data 2 output
	JRSOUT1	TS parallel data 1 output
	JRSOUT0	TS parallel data 0 output
PSK (Synchronized with TS serial)	JSRCK	TS serial clock output
	JSRDT	TS serial data output
	JRSCKO	TS byte clock output
	JSBYTE	TS synchronization byte flag output
	JPBVAL	TS (packet) valid flag output
	JRSEORF	RS decoding error (packet) flag output
	JSTSFLG1	Status register output 1
	JSTSFLG0	Status register output 0 (Emergency alarm broadcasting start flag dedicated)
	JLOCK	Super frame synchronization flag
	JPORT	General-purpose port output (or LNB power supply control output)

By default, the following pin assignments are made:

PSK (TS) serial signal: System C pins

PSK (TS) parallel signal: System D pins

[The OFDM (TS) parallel signals are assigned to System A pins, and OFDM (TS) serial signals are assigned to System B pins.]

PSK signals can be assigned to pins other than the default pins by using two-stage setting.

First select (set to "3") the PSK signal system using the OFDM registers pinsla, pinslb, pinslc, and pinsld, and then select PSK serial or PSK parallel using the PSK signal system selection registers jtsla, jtslb, jtslc, and jtsld.
At this time, pinsla, pinslb, pinslc, and pinsld correspond to Pin System A, B, C, and D, respectively. Similarly, jtsla, jtslb, jtslc, and jtsld correspond to Pin System A, B, C, and D, respectively. Use the registers of the Pin System to be set.

8.3.3 Enable Control of Output Signal

The output enabled/disabled (High-Z or pull-down) initial state can be switched using the JOEN pin. Output is enabled when JOEN="0" and disabled when JOEN="1." The JOEN pin setting is captured into the IC when SYRSTN is "0" and confirmed when SYRSTN changes from "0" to "1."
In addition, the enabled / "High-Z" or "pull-down"/ fixed to "0" / fixed to "1" state can be individually set by setting the register (address 1CH, 1Dh, 1Eh or 1Fh) corresponding to the output signal.

* The pin name and the signal name output to the pin are expressed in uppercase characters, but the signal name differs from the pin when the output pin is switched. Your attention should be given to this. For example, because the PSK serial/synchronization signal is output to System C by default, the JSTSFLG1 signal is output to the JSTSFLG1 pin, but when the assignment is changed to another pin system, the JSTSFLG1 signal is output from a pin other than JSTSFLG1.
* The JOEN control setting, register based enabled setting and polarity inversion setting are performed against signals, not pins. Thus, these settings do not need to be changed when pin assignments are changed.
* High-Z and pull-down are specified for each pin individually. Refer to Chapter 4 "Pin Functions."

8.3.4 Status Register

The contents of the status registers (addresses C3h) and emergency alarm broadcast start flag emgcy can be output to the JSTSFLG1 and JSTSFLG0 signals.

(1) Status register 1

This status register is output as the logical sum of the signals selected by the enable setting register (address 1Ah) from the 8 bits of status information described below. The same flag as for status register 1 is output for the JSTSFLG1 signal.

inpnon:	Monitors the input signal level ("1" when the input signal level is too low).
unlock:	Monitors the demodulation synchronization and super frame synchronization status ("1" when the asynchronous mode is assumed).
crslip:	Monitors the carrier recovery cycle slip ("1" when a cycle slip occurs).
tmcerr:	Monitors TMCC modulation errors ("1" when an error occurs).
sdive:	Monitors TMCC site diversity instructions ("1" when an instruction is issued).
rlockl:	Monitors low-layer RS demodulation error ("1" when no error is found, "0" when no layer is found).
tmcrev:	Monitors TMCC1 extension flags ("1" when an extension flag is present).
tmchg:	Monitors the TMCC change flag ("1" when there is a change in bit 5 of the change flag).

The output format of the JSTSFLG1 signal can be selected so that output changes to "1" at the "0" to "1" or "1"to "0" change point using register jstmdd. Note that the JSTSFLG1 pin is reset to "0" by resetting an arbitrary value to the jstmdd register.

(2) Status register 0

The emergency alarm broadcast start flag signal emgcy can be output as a JSTSFLG0 signal.

emgcy:	TMCC emergency alarm broadcast start flag ("1" when start control is provided)

Note that once emgmsk="1" is set, JSTSFLG0 is not output even when an emergency alarm broadcasting start flag is detected if all the layers of the selected TS contain an error. The same applies to monitoring of the startup control signal (with startup control provided). (Refer to Section 8.2.3.)
The output format of the JSTSFLG0 signal can be selected so that output changes to "1" at the "0" to "1" or "1"to "0" change point using register jstmdc. Note that the JSTSFLG0 signal is reset to "0" by resetting an arbitrary value to the jstmdc register.

8.3.5 Error Free Flag

The high layer RS post-correction error free flag signal can be output as a JRLOCKH signal. In addition, the low layer RS post-correction error free flag signal rlockl can be output as a JRLOCKL signal.
The output format of the JRLOCKL and JRLOCKH1 signals can be selected so that output changes to "1" at the "0" to "1" or "1" to "0" change point using the jstmda and jstmdb registers. Note that the JRLOCKL and JRLOCKH signals are reset to "0" by resetting an arbitrary value to the stmda and jstmdb registers.

8.3.6 Super Frame Synchronization Flag

A flag to indicate detection of a super frame synchronization during ISDB-S transmission can be output JLOCKL and JLOCKH signals. (The output format at change points cannot be selected for this flag.)

8.3.7 Layer Identification Flag

JRLOCKH and JRLOCKL signals can be switched to the layer identification signals JHSEL1 and JHSEL0 shown below by setting "1" to the jhselout register. JHSEL1 contains higher bits and JHSEL0 contains lower bits to identify a layer and null for each packet as shown below:

Layer Identification Flag Output when the jhselout Register="1"

JHSEL1 (JRLOCKH pin)	JHSEL0 (JRLOCKL pin)	Identified layer
0	0	Unused
0	1	High-layer packet
1	0	Low-layer packet
1	1	Null packet (excluding transmission null packets.)

8.3.8 LNB Tone Control Output

A tone (TONE) signal can be output for control of LNB (Low Noise Block down converter). The TONE signal is a pulse wave with a frequency of MD/1792 and a duty ratio of 50%. When MD=76.2 MHz, for example, the tone frequency is 42.5 kHz.

Name	Address (HEX)	Data	R/W	Initial Value	Description
iqch	06	[6]	W	0x0	IQ change selection 0: Do not change, 1: Change.
bytesel	06	[3]	W	0x0	JSBYTE output switching Switches synchronization output from the JSBYTE pin 0: TS packet synchronization, 1: Frame synchronization
jhselout	06	[2]	W	0x0	Switching of the JRLOKCH and JRLOCKL pins 0: JRLOKCH, JRLOCKL 1: JHSEL1, JHSEL0
jtsld	07	[6]	W	0x1	PSK system signal output selection (PSK parallel output pin) 0: Serial output/synchronization, 1: Parallel output
jtslc	07	[4]	W	0x0	PSK system signal output selection (PSK serial output pin) 0: Serial output/synchronization, 1: Parallel output

jtslb	07	[2]	W	0x0	PSK system signal output selection (PSK serial output pin) 0: Serial output/synchronization, 1: Parallel output
jtsla	07	[0]	W	0x1	PSK system signal output selection (OFDM parallel output pin) 0: Serial output/synchronization, 1: Parallel
lnb	14	[6]	W	0x0	TONE output (JLNB pin) setting (blnb_en setting has a high priority.) 0: OFF (fixed to "0") 1: ON
jport	14	[5]	W	0x0	Output port (JPORT pin) setting 0: Fixed to "0" 1: Fixed to "1" *When register atpt is set to "1," the port setting of JPORT becomes disabled and a standby operation interlock is set.
inpnone	1A	[7]	W	0x0	Status register 1 inpnon enable 0: Disable, 1: Enable
unlocke	1A	[6]	W	0x0	Status register 1 unlock enable 0: Disable, 1: Enable
crslipe	1A	[5]	W	0x0	Status register 1 crslip enable 0: Disable, 1: Enable
tmcerre	1A	[4]	W	0x0	Status register 1 tmcerr enable 0: Disable, 1: Enable
sdivee	1A	[3]	W	0x0	Status register 1 sdive enable 0: Disable, 1: Enable
rlockle	1A	[2]	W	0x0	Status register 1 rlockl enable 0: Disable, 1: Enable
tmcreve	1A	[1]	W	0x0	Status register 1 tmcrev enable 0: Disable, 1: Enable
tmchge	1A	[0]	W	0x0	Status register 1 tmchg enable 0: Disable, 1: Enable
inpnoneiv	1B	[7]	W	0x0	Status register 1 inpnon polarity inversion 0: Normal, 1: Inversion
unlockeiv	1B	[6]	W	0x0	Status register 1 unlock polarity inversion 0: Normal, 1: Inversion
crslipeiv	1B	[5]	W	0x0	Status register 1 crslip polarity inversion 0: Normal, 1: Inversion
tmcerreiv	1B	[4]	W	0x0	Status register 1 tmcerr polarity inversion 0: Normal, 1: Inversion
sdiveeiv	1B	[3]	W	0x0	Status register 1 sdive polarity inversion 0: Normal, 1: Inversion
rlockleiv	1B	[2]	W	0x0	Status register 1 rlockl polarity inversion 0: Normal, 1: Inversion
tmcreveiv	1B	[1]	W	0x0	Status register 1 tmcrev polarity inversion 0: Normal, 1: Inversion
tmchgeiv	1B	[0]	W	0x0	Status register 1 tmchg polarity inversion 0: Normal, 1: Inversion
bpbv_en [1:0]	1C	[7:6]	W	JOEN	JPBVAL signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"
brse_en [1:0]	1C	[5:4]	W	JOEN	JRSEORF signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"

bstf1_en [1:0]	1C	[3:2]	W	JOEN	JSTSFLG1 signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"
bstf0_en [1:0]	1C	[1:0]	W	JOEN	JSTSFLG0 signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"
bstat_en [1:0]	1D	[7:6]	W	JOEN	JRLOCKH signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"
block_en [1:0]	1D	[5:4]	W	JOEN	JLOCK signal output control 0 or JOEN="0": Enable 1 or JOEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
bstatl_en [1:0]	1D	[3:2]	W	JOEN	JRLOCKL signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (3-state output buffer: High-Z state, pull-down) 2: Fixed to "0" 3: Fixed to "1"
brso_en [1:0]	1D	[1:0]	W	JOEN	JRSOUT7 to JRSOUT0 signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (3-state output buffer: High-Z state, pull-down) 2: Fixed to "0" 3: Fixed to "1"
bpot_en [1:0]	1E	[5:4]	W	JOEN	JPORT signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"
bagc_en [1:0]	1E	[3:2]	W	JOEN	JAGCCNT signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (3-state output buffer: High-Z state, pull-down) 2: Fixed to "0" 3: Fixed to "1"
blnb_en [1:0]	1F	[7:6]	W	JOEN	JLNB signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (3-state output buffer: High-Z state, pull-down) 2: Fixed to "0" 3: Fixed to "1"
bsrf_en [1:0]	1F	[5:4]	W	JOEN	JSRCK/JSRDT signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"
brsck_en [1:0]	1F	[3:2]	W	JOEN	JRSCKO signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"

bsby_en [1:0]	1F	[1:0]	W	JOEN	JSBYTE signal output control 0 or JOEN="0": Enable 1 or JOEN="1": Disable (High-Z) 2: Fixed to "0" 3: Fixed to "1"
jstmdd [1:0]	20	[7:6]	W	0x0	JSTSFLG1 signal output mode setting 0: Normal flag ("1" when conditions occur) 1: Output "1" at "0" to "1" change point 2: Output "1" at "1" to "0" change point 3: Output "1" at either change point (Flag reset at writing of value other than 0)
jstmdc [1:0]	20	[5:4]	W	0x0	JSTSFLG0 signal output mode setting 0: Normal flag ("1" when conditions occur) 1: Output "1" at "0" to "1" change point 2: Output "1" at "1" to "0" change point 3: Output "1" at either change point (Flag reset at writing of value other than 0)
jstmdb [1:0]	20	[3:2]	W	0x0	JRLOCKH signal output mode setting 0: Normal flag ("1" when conditions occur) 1: Output "1" at "0" to "1" change point 2: Output "1" at "1" to "0" change point 3: Output "1" at either change point (Flag reset at writing of value other than 0)
jstmda [1:0]	20	[1:0]	W	0x0	JRLOCKL signal output mode setting 0: Normal flag ("1" when conditions occur) 1: Output "1" at "0" to "1" change point 2: Output "1" at "1" to "0" change point 3: Output "1" at either change point (Flag reset at writing of value other than 0)
inpnon	C3	[7]	R	0xX	Status register 1 flag inpnon Flag for monitoring the presence of input signals 0: Input signal level normal 1: Input signal level too low
unlock	C3	[6]	R	0xX	Status register 1 flag unlock 0: Synchronization normal 1: Out of frame synchronization and demodulation
crslip	C3	[5]	R	0xX	Status register 1 flag crslip 0: No carrier recovery cycle slip 1: Carrier recovery cycle slip
tmcerr	C3	[4]	R	0xX	Status register 1 flag tmcerr 0: No TMCC decoding error 1: TMCC decoding error
sdive	C3	[3]	R	0xX	sdive flag of status register 1 0: No TMCC site diversity switching 1: TMCC site diversity switching in progress
emgcy	C3	[2]	R	0xX	emgcy flag of status register 0 0: No TMCC emergency alarm broadcast start flag 1: TMCC emergency alarm broadcast start flag
tmcrev	C3	[1]	R	0xX	tmcrev flag of status register 1 0: No TMCC extension flag 1: TMCC extension flag
tmchg	C3	[0]	R	0xX	tmchg flag of status register 1 0: No change in TMCC change instruction flag 1: Change in TMCC change instruction flag
pm1d	C5	[7:3]	R	0xX	TMCC change instruction information monitor The 5 bits of the TMCC change instruction flag are incremented by 1 each time a change is made to the TMCC information and return to "00000" after reaching "11111."
rlockh	C5	[1]	R	0xX	High-layer RLOCK monitor 0: RS decoding error, 1: No RS decoding error
rlockl	C5	[0]	R	0xX	Low-layer RLOCK monitor 0: RS decoding error, 1: No RS decoding error (Also "0" when layers do not exist)

* JOEN: Determined by the JOEN pin setting at power-on reset and when the isyrst register is set.

8.4 Clock Recovery

TC90512 resamples the I and Q signals synchronous with the PSK symbol timing.

8.4.1 Clock Frequency Offset Correction

The value found using the following equation based on the master clock frequency MD and PSK symbol rate JFS is set in hkfrq.

$$jhkfrq = ((MD / JFS) - 2) \times 2^{15} \quad \text{(Equation 8-4-1)}$$

Calculation example: Master clock frequency MD=76.2 [MHz], BS 8PSK symbol rate JFS=28.86 [MHz]

$$jhkfrq[15:0] = (76.2 / 28.86 - 2) \times 2^{15}$$
$$\fallingdotseq 20{,}982\ (51F6h)$$

8.4.2 Clock Frequency Error Monitor

The clock frequency error from register clkfrq is found from the equation below. clkfrq is an 8-bit 2's complement expression.

$$\text{Clock frequency error [ppm]} = clkfrq \times JFS[MHz] / MD \times 7.63 \quad \text{(Equation 8-4-2)}$$

Calculation example: clkfrq[7:0]=14h (+20dec), BS 8PSK symbol rate JFS=28.86 [MHz],
Master clock frequency MD=76.2 [MHz]

$$\text{Clock frequency error} = (+20) \times 28.86/76.2 \times 7.63$$
$$= +58\ [ppm]$$

Name	Address (HEX)	Data	R/W	Initial Value	Description
jhkfrq [15:8]	0C	[7:0]	W	XSEL	Set the clock recovery offset frequency. hkfrq = ((MD / JFS) - 2) x 2^{15} Although the setting range is 0400h to FBFFh, basic frequency setting is carried out automatically by XSEL1 and XSEL0.
jhkfrq [7:0]	0D	[7:0]	W	XSEL	
clkfrq [7:0]	BE	[7:0]	R	0xXX	Clock frequency error monitor 2's complement expression. Clock frequency error can be calculated using the following equation: Frequency error [ppm] = clkfrq x JFS[MHz] /MD[MHz] x 7.63 JFS (symbol rate) = 28.86 [MHz]

* XSEL: For more information about automatic setting by XSEL, refer to Sections 6.5 and 10.

8.5 AGC

(1) DAC operation clock frequency setting

The AGC control output of the tuner is in 1-bit DAC format with the amplitude resolution equivalent to 12 bits.
The DAC operation clock frequency can be set by register aagpcw[1:0]. The higher the DAC operation clock frequency, the higher the pulse harmonics frequency, thus making it possible to use a simplified LPF. However, note the spurious caused by harmonics. When implementing the IC, insert resistors of 10 to 20 kΩ in series near the AGC control output pin.

Table 8.1 Setting the DAC Operation Clock Frequency

aagpcw[1:0]	DAC Operation Clock Frequency [MHz]
0	MD/32
1	MD/16
2	MD/8
3	MD/4

MD: Master clock frequency [MHz]

(2) Adaptive input level control

AGC control of the TC90512 PSK demodulator performs adaptive control in accordance with input signal noise amplitude. The acolvl register sets the threshold value of AGC error coring for improvement of low C/N characteristic.

(3) Correcting AGC control characteristics

TC90512 AGC control output characteristics can switch two gains (aagcdv and aagcdv x aggsft) with aggthr set as the change point so that the nonlinear characteristics of tuner AGC control sensitivity can be corrected approximately. If these gains approximate the nonlinear characteristics of AGC control sensitivity, the loop gain as a total gain can be virtually set to a constant value. The aggthr is the register that sets the gain changeover points, setting the full range of AGC control signals based on 16 levels. The aagcdv is the register that sets the normal control gains, setting the value based on 8 levels. The gains after the changeover point are aagcdv x aggsft; aggsft can be set at four levels (x8, x4, x2, x1).
Furthermore, the agcgn register can also be used for normal control gain adjustment. While aagcdv increases the gain by the power of two, agcgn conversely decreases the gain by the power of two. These total gains are the gains when aggthr is the gain changeover point or less.

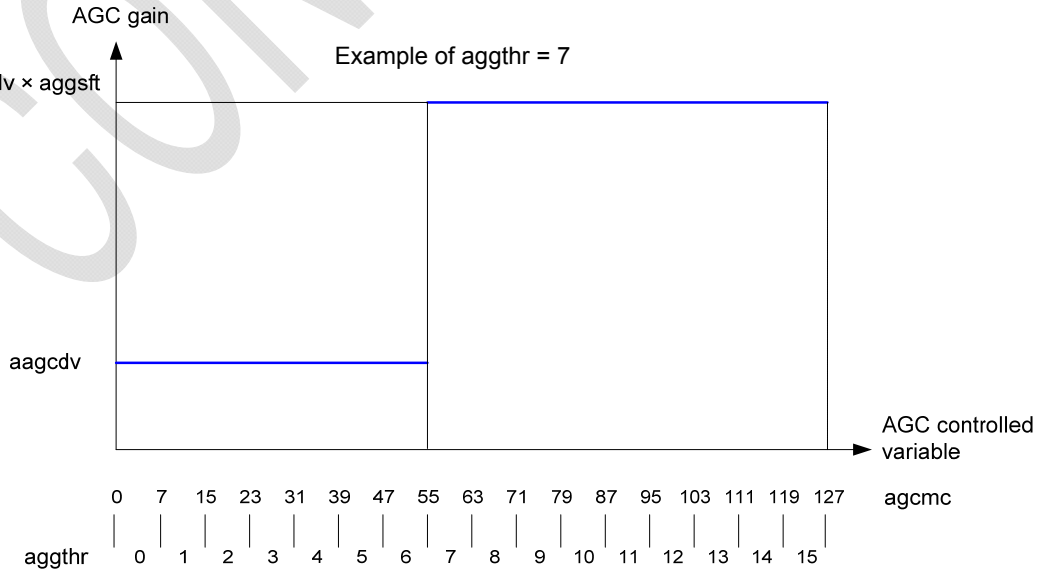


Figure 8.2 Correcting the AGC Control Characteristics

(4) AGC control output limiter

AGC control output can be limited by the upper/lower limiter. The lower limit of the control output can be set by the aglmin register. The upper limit of the control output can be set by the aglmax register. Either setting is made in straight binary format of 0 to 255.

Name	Address (HEX)	Data	R/W	Initial Value	Description
aglmin [7:0]	09	[7:0]	W	0x00	AGC control output lower limit setting Sets the value in straight binary format. 0: Minimum value to 255: Maximum value
aglmax [7:0]	0A	[7:0]	W	0xFF	AGC control output upper limit setting Sets the value in straight binary format. 0: Minimum value to 255: Maximum value
agcgn [2:0]	0E	[2:0]	W	0x0	AGC control gain adjustment Sets the gain based on the power of two. 0: Maximum to 7: Minimum
aagcdv [2:0]	10	[5:3]	W	0x6	AGC control gain adjustment Sets the gain based on the power of two. 0: Maximum to 7: Minimum
amglvl [9:8]	10	[1:0]	W	0x2	AGC control output initial value setting (Upper) (Lower) 0: Minimum to 1023: Maximum
amglvl [7:0]	11	[7:0]	W	0x00	
aagpcw [1:0]	12	[7:6]	W	0x0	DAC operation clock frequency setting 0:MD/32, 1:MD/16, 2:MD/8, 3:MD/4
aggsft [1:0]	12	[5:4]	W	0x3	Nonlinear compensation gain of AGC control sensitivity Sets the gain of the aggthr changeover point and thereafter to aagcdv x aggsft. 0: x8, 1: x 4, 2: x 2, 3: x 1
aggthr [3:0]	12	[3:0]	W	0x0	Nonlinear compensation changeover point of AGC control sensitivity 0: Minimum value to 15: Maximum value
acolvl [7:0]	38	[7:0]	W	0x40	AGC error detection coring threshold value setting Ignores low-amplitude error signals, improving low C/N characteristics. 0: Minimum to 255: Maximum
aagref [7:0]	39	[7:0]	W	0x10	AGC input reference level setting 0: Minimum to 255: Maximum
aagcinv	87	[2]	W	0x0	AGC control polarity 0: Normal, 1: Inversion
agcmc [6:0]	BA	[6:0]	R	0xXX	AGC control volume monitor output 0: Minimum value to 127: Maximum value

8.6 Carrier Recovery

8.6.1 Carrier AFC Loop Gain Setting

The carrier AFC loop gain changes according to the PSK symbol rate JFS and master clock frequency MD. Thus, set the value found by the following equation in register afcg.

afcg = (JFS / MD) x 214 + 1 (Equation 8-6-1)

Calculation example: Master clock frequency MD=76.2[MHz], PSK symbol rate JFS=28.86[MHz]
afcg = (28.86 / 76.2) x 214 + 1
≒82
= 52h

TC90512 performs optimum control by switching the carrier recovery loop gain automatically in accordance with 8PSK, QPSK, and BPSK modulation. The loop gains of QPSK and BPSK modulation are set to the pllqhgd and pllbhgd registers, respectively. In addition, the upper limit value for PLL loop gain control in adaptive control is set to pllhmax.

8.6.2 Carrier Frequency Error Monitor

The carrier frequency error can be monitored by the afcfrq register. The afcfrq is a 2's complement expression.

Carrier frequency error [MHz] = afcfrq x master clock frequency MD [MHz] ÷1024 (Equation 8-6-2)

Calculation example: When afcfrq[7:0] = 17h (+23dec)
Carrier frequency error = (+23) x 76.2/1024
= +1.712[MHz]

* In this calculation example, the carrier frequency of the input signal is 1.712 MHz higher than the tuner local oscillator frequency. Conversely, when the number obtained from the above equation is negative, the carrier frequency of the input signal is lower than that of the tuner local oscillator.

Name	Address (HEX)	Data	R/W	Initial Value	Description
afcg [7:0]	0F	[7:0]	W	XSEL	Carrier recovery AFC gain setting Sets the value found by the following equation. afcg = (JFS/MD) x 214＋1 1: Minimum to 255: Maximum
pllhmax[3:0]	51	[7:4]	W	0xC	Carrier PLL time constant automatic control range upper limit setting 11: Minimum to 15: Maximum
pllbhgd[5:4]	52	[1:0]	W	0x2	BPSK direct gain setting for carrier PLL stationary period 0: Minimum to 63: Maximum
pllbhgd[3:0]	53	[7:4]	W	0x1	
pllqhgd[5:4]	5A	[1:0]	W	0x2	QPSK area direct gain setting for carrier PLL stationary period 0: Minimum to 63: Maximum
pllqhgd[3:0]	5B	[7:4]	W	0x2	
afcfrq [7:0]	BB	[7:0]	R	0xXX	Carrier frequency error monitor Indicates the carrier frequency error. 2's complement expression. -128: Minimum to 127: Maximum

* XSEL: For more information about automatic setting by XSEL, refer to Sections 6.5 and 10.

8.7 Synchronization

TC90512 contains the demodulation synchronization control circuit, eliminating the need for external control. The carrier asynchronous status can be monitored by crunlock.

Name	Address (HEX)	Data	R/W	Initial Value	Description
crunlock	BA	[7]	R	0xXX	Carrier asynchronous monitor Indicates the synchronous state of the demodulation section. 0: Synchronized, 1: Not synchronized

8.8 Equalization

8.8.1 Equalizer

The IC adaptively eliminates signal distortion caused by cable reflection and other, in accordance with the input conditions. TC90512 contains the control circuit, eliminating the need for external control.

8.8.2 C/N Estimation

It is possible to estimate the C/N value of the input signal from the demodulation S/N. The approximate input signal C/N (dB value) can be found by replacing the value of the cnmc register in the following equation.

$$C/N[dB] = -1.6346 \times P^5 + 14.341 \times P^4 - 50.259 \times P^3 + 88.977P^2 - 89.565 \times P + 58.857 \quad \text{(Equation 8-8-1)}$$

Where $P=(cnmc - 3000)^{1/2} \div 64$ and cnmc is 3000 or higher

While the C/N range in which estimation is possible from the approximation equation above is 0 to 30dB, signal processing deterioration is included as well. Be sure to use the formula for reference purposes only. A simpler approximation equation is as follows.

$$C/N[dB] = -0.14 \times (cnmc - 3000)^{1/2} + 28.7 \quad \text{(Equation 8-8-2)}$$

Where cnmc is 3000 or higher.

In this case, the C/N range in which estimation is possible is 6 to 17 dB. When the value is outside of this range, the error margin becomes larger.

Name	Address (HEX)	Data	R/W	Initial Value	Description
deqoff	3B	[0]	W	0x0	Equalizer factor clear (for test) 0: Equalization operation, 1: Clear equalizer factor
cnmc [15:8]	BC	[7:0]	R	0xXX	C/N monitor (Upper) (Lower) Straight binary format. Indicates that the greater the value, the higher the noise level. (Phase noises are excluded.)
cnmc [7:0]	BD	[7:0]	R	0xXX	

8.9 Error Correction

8.9.1 TS Output Settings

The various TS output settings can be set by the registers described below.

1) TS output format

Register dvaloff:	Sets the parity period of TS parallel and serial output data to "0."
Register pkstop:	Stops the parity period TS serial clock.
Register rsckrev:	Inverts the TS parallel output clock polarity.
Register chclkp:	Inverts the TS serial output clock polarity.
Register oponff:	Forcibly changes the high layers to a null packet.

2) Valid flag related

Register nuval:	Sets the null packet valid flag off (excluding null packets actually transmitted).
Register anuval:	Does not set the valid signal of packets forcefully or automatically nullified when nuval = "1."
Register valrev:	Inverts the valid polarity.

3) Error flag related

Register msboff:	Turns OFF the RS decoding error bit (2nd byte MSB) addition of the TS packet header. Used for BER measurement at TS packet output.
Register asyncng:	Turns OFF the function that sets all the TS packets (including null packets) error during the asynchronous period until demodulation pull-in completes.

8.9.2 TS_ID Setting of Output TS

The TS_ID of output TS is specified by the iits register. When the specified TS_ID does not exist in received data, the TS data that exists in the first slot of the transmission frame is output automatically.

8.9.3 TMCC Information Output

With the tmccadd register set to "1" for a test purpose, the TS header can be replaced by TMCC information (48 bytes). The location of replacement is slots 2 to 9 of slots 0 to 47 in frames 0 to 5 of frames 0 to 7. All other locations are left as the normal 47h header as is.
With the bytesel register set to "1," the signal is changed to the JSBYTE signal (TS packet synchronization of PSK demodulation TS output), enabling super frame synchronization output. This can be used for synchronization of the above TMCC information.

8.9.4 Serial Output for BER Measurement

Setting the beron register to "1" outputs the serial data and clock for BER measurement instead of the serial TS output. For layer modulation, TS layers are selected by the hlmask register, making it possible to output the BER serial data and clock for each layer. Before this measurement is conducted, PRBS (pseudo random binary sequence) needs to be sent as data to the transmitter.
Furthermore, because the PRBS sequence is not transmitted during the dummy slot period generated for each transmission mode, parity section and synchronous 47h header, BER data are not output from the BER measurement pin during that period. The BER measurement clock also stops.

8.9.5 RS Decoding ON/OFF

RS decoding for the main signal and TMCC signal can be turned ON/OFF. The main signal is turned ON/OFF by the rsoff register, and the TMCC signal is turned ON/OFF by the tmoff register.

8.9.6 Error Rate Measurement after Viterbi Decoding

With the corchh register set to "1," the number of error bits corrected in RS decoding can be counted for each set cycle for the TS selected by the iits register.
When the number of bits corrected by RS decoding can be approximated as equal to the number of error bits after Viterbi correction (or when errors are relatively few in number), the number of error bits divided by the total number of bits in the measurement cycle is the BER value after Viterbi correction.

1) Selecting the measurement cycle mode

In ISDB-S, the number of slots per super frame differs for each TS and layer. Two measurement cycle modes are therefore provided: "slot mode" which specifies the total number of slots, and "time mode" which specifies the number of super frames.

Slot mode:	tschh="0" Counts the number of errors (number of error bits when corchh = "1") for each specified number of slots.
Time mode:	tschh="1" Counts the number of errors (number of error bits when corchh = "1") for each set number of super frames.

2) Selecting the BER measurement layer

For BER measurement using the TC90512-contained error counter, layer selection is not required since errors can be counted on two layers simultaneously. For measurement using an external BER counter, however, the layer to be measured must be set by the hlmask register. Note that, for single layer transmission, measurement is performed on the high layer side.

High layer or single layer BER measurement:	hlmask[1:0] = "10"
Low layer BER measurement:	hlmask[1:0] = "01"

3) Setting the measurement cycle

The measurement cycle for both slot mode and time mode are set in registers below.

High layer or single layer measurement cycle:	Sets the number of slots or number of super frames in cych[2:0].
Low layer measurement cycle:	Sets the number of slots or number of super frames in cycl[2:0].

4) Reading the error count (number of bits)

High layer or single layer count value:	Output to perrh[23:0]
Low layer count value:	Output to perrl[23:0]

5) Reading the total number of packets of the measurement cycle

The number of slots specified in slot mode is the same as the number of packets. In time mode, however, the number of slots (number of packets) in one super frame differs depending on transmission parameters. The total number of packets of the period of the number of super frames specified by cych or cycl can be read using the following registers:

Total number of packets of high layer or single layer:	Output to pecyh[15:0]
Total number of packets of low layer:	Output to pecyl[15:0]

6) Calculating BER after Viterbi decoding

The following equations can be used to approximately calculate BER after Viterbi decoding:

High-layer BER ≒ perrh / (pecyh x 204 x 8) (Equation 8-9-1)
Low-layer BER ≒ perrl / (pecyl x 204 x 8) (Equation 8-9-2)

* The number of error bits cannot be identified when errors of 9 bytes or more exist but correction by RS decoding is not possible. For this reason, the approximate calculation result of the equation shown above is saturated at about 7.8×10^{-2}.

8.9.7 Error Rate Measurement after RS Decoding

With the corchh register set to "0" (default), the number of error packets (the number of packets with errors of 9 bytes or more that cannot be corrected by RS) after RS decoding can be counted for each setting period for the TS selected by the iits register.
The packet error rate PER is calculated based on the ratio of the number of packets that cannot be corrected by RS to the total number of packets of the measurement cycle. At this time, BER is calculated on the supposition that the number of error bytes in a packet that cannot be corrected by RS is nine. (The probability of occurrence of an error of 10 bytes or more is presumed to be low.)

1) Selecting the measurement cycle mode

In ISDB-S, the number of slots per super frame differs for each TS and layer. Two measurement cycle modes are therefore provided: "slot mode" which specifies the total number of slots, and "time mode" which specifies the number of super frames.

Slot mode:	tschh="0" Counts the number of errors (number of error packets when corchh = "0") for each specified number of slots.
Time mode:	tschh="1" Counts the number of errors (number of error packets when corchh = "0") for each specified number of super frames.

2) Selecting the BER measurement layer

For BER measurement using the TC90512-contained error counter, layer selection is not required since errors can be counted on two layers simultaneously. For measurement using an external BER counter, however, the layer to be measured is set by the hlmask register. Note that, for single layer transmission, measurement is performed on the high layer side.

High layer or single layer BER measurement:	hlmask[1:0] = "10"
Low layer BER measurement:	hlmask[1:0] = "01"

3) Setting the measurement cycle

The measurement cycle for both slot mode and time mode are set in the registers below.

High layer or single layer measurement cycle:	Sets the number of slots or number of super frames in cych[2:0].
Low layer measurement cycle:	Sets the number of slots or number of super frames in cycl[2:0].

4) Reading the error count (number of packets)

The error count (number of packets) is read by the following register.

High layer or single layer count value:	Output to perrh[23:0]
Low layer count value:	Output to perrl[23:0]

5) Reading the total number of packets of the measurement cycle

The number of slots specified in slot mode is the same as the number of packets. In time mode, however, the number of slots (number of packets) in one super frame differs depending on transmission parameters. The total number of packets of the period of the number of super frames specified by cych or cycl can be read using the following registers:

Total number of packets of high layer or single layer:	Output to pecyh[15:0]
Total number of packets of low layer:	Output to pecyl[15:0]

6) Calculating BER after RS decoding

The following formula can be used to approximately calculate BER after RS decoding.

High-layer PER ≒ perrh / pecyh (Equation 8-9-3)
High-layer BER ≒ (perrh x 8 x 0.5 x 9) / (pecyh x 204 x 8) (Equation 8-9-4)

Low-layer PER ≒ perrl / pecyl (Equation 8-9-5)
Low-layer BER ≒ (perrl x 8 x 0.5 x 9) / (pecyl x 204 x 8) (Equation 8-9-6)

* When RS correction is not possible, the number of error packets cannot be specified. A margin of error is therefore included.

8.9.8 Setting for Changing TS Output Packets to Null Packets at Hierarchical Modulation

(1) High layer forced null setting

With the oponff register set to "1," the high layer packet of the output TS can be forcibly replaced by a null packet.

(2) Automatic null packet replacement at frequent error occurrence

When error packets frequently occur, malfunction due to TS_ID misidentification, etc., may occur in the MPEG decoder. TC90512 prevents such malfunctions by automatically replacing TS packets with null packets in accordance with the error occurrence frequency.

1) Setting the error count mode

When automatic null packet replacement is to be used, set corchh to "0" (counts errors based on the number of packets).

2) Setting the measurement cycle mode

Similar to the operation performed for BER measurement, select slot mode (packet unit) or time mode (super frame unit).Note that the counter used for error measurement can be reset by jperst.

3) Setting the measurement cycle

Similar to the operation performed for BER measurement, set the cycle for error counting to the cych and cycl registers.

4) Specifying the layer for automatic null packet replacement

Automatic null packet replacement can be set for the high layer and low layer, individually. The setting is set for the high and low layers by setting the nullon_h (high layer) and nullon_l (low layer) registers to "1," respectively.

5) Setting the automatic null packet replacement ON/OFF threshold value

Set the threshold value for the error count. When this threshold value is exceeded, the TS output packet is replaced with a null packet. Hysteresis characteristics can be applied to the threshold value. The threshold value for deciding "null packet replacement ON" is set in shcl[2:0] when the error count value increases, and the threshold value for deciding "null packet replacement OFF" is set in shch[2:0] when the error count value decreases. To ensure that the hysteresis operation is properly performed, set the values so that shcl≤shch. These threshold values are common to the high layer and low layer.

* The threshold values shch and shcl are set based on the ratio to the number of packets of the observation packet cycle pecyh or pecyl. Set the values so that the product with the observation packet cycle is 1 or greater. For instance, when the observation cycle is "384 packets" in slot mode and the settings are made so that shch or shcl are "1/512 of the cycle," the products shch x pecyh (or pecyl) or shcl x pecyh (or pecyl) are less than 1 packet even if an error occurs in all packets, causing improper operation.
* The assessment result of the threshold value can be checked by register nul_h or nul_l.

8.9.9 Setting the RS Decoding Error Flag JRLOCK

Information regarding whether or not an error is present in an RS decoded TS packet (only the high layer of TS selected by TS_ID) can be output to the JRLOCK flag. Although the RSEORF signal is a TS packet unit error flag, JRLOCK determines error presence based on a longer observation period.
The JRLOCK decision criteria are as follows: the flag is set with continuous error free TS packets and not set with continuous error TS packets. The number of continuous TS packets required to make the decision is set in the okval[2:0] and erval[2:0] registers, respectively.

Number of continuous error TS packets for JRLOCK

okval/erval	No. of Assessed Packets
0	1 (erval default value)
1	2
2	4
3	8
4	16
5	32
6	64
7	128 (okval default value)

Furthermore, when a layer-transmitted TS is selected, JRLOCK indicates the decision results pertaining to error presence in high layers only. okval and erval, however, are commonly used for both high and low layers and related decision results can be monitored using the rlockh and rlockl registers, respectively.

8.9.10 Relationship of Error Decision , BER Measurement and Null Packet Replacement

Figure 8.3 shows the relationship between the error flags, BER measurement, and null packet replacement settings. JRSEORF indicates the continuous error decision result of high-layer TS packets. In addition, the rlockl register indicates the continuous error decision result of low-layer TS packets. (rlockl can be output to the STSFLG1 pin.)
The JRLOCK and rlockl results can be reflected in JRSEORF, the final TS packet error flag. This enables suppression of the JRSEORF unstable state (a state where the TS error flag alternately changes to 1 and 0 in the synchronization pull-in process). On the other hand, BER measurement and the null packet replacement process use the error counter result. In conjunction with null packet replacement, the valid signal can also be linked using nuval and anuval.
Note that error free decision on the low layer is slower than that on the high layer because the TS transmission rate of the low layer is low.

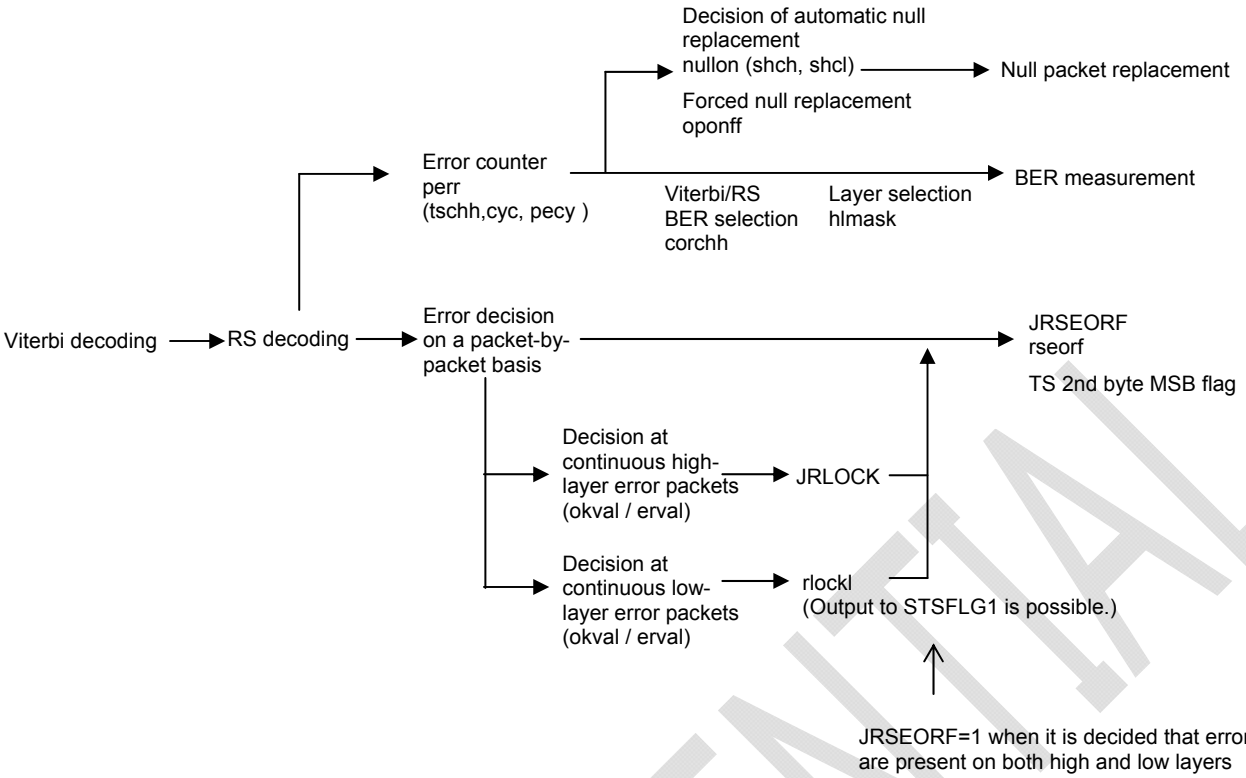


Fig. 8.3 Setting the Error Flag

Name	Address (HEX)	Data	R/W	Initial Value	Description
chclkp	04	[1]	W	0x0	JSRCK output polarity inversion Inverts the clock polarity output from the JSRCK output pin. 0: Normal, 1: Inversion
rsoff	8D	[7]	W	0x0	RS decoding operation setting for main signal 0: ON, 1: OFF (for test)
tmoff	8D	[6]	W	0x0	RS decoding operation setting for TMCC signal 0: ON, 1: OFF (for test)
msboff	8D	[5]	W	0x0	TS packet 2nd MSB error flag setting 0: Set to 1 with error (normal) 1: Flag not changed (for BER measurement by external counter)
nullon_h	8D	[3]	W	0x0	High-layer automatic null replacement setting 0: OFF, 1: ON
nullon_l	8D	[2]	W	0x0	Low-layer automatic null replacement setting 0: OFF, 1: ON
tmccadd	8D	[1]	W	0x0	TMCC information insertion Replaces the TS packet synchronization byte (47h) with TMCC information (48 bytes). 0: Do not replace with TMCC information (normal) 1: Replace with TMCC information (for a test purpose)
hlmask [1:0]	8E	[7:6]	W	0x0	BER measurement layer selection 00: Normal (other than BER measurement) 01: Low layer BER measurement 10: High layer or single layer BER measurement 11: Undefined
dvaloff	8E	[5]	W	0x0	Sets the TS parallel and serial parity period to "0" 0: Do not set the parity period data to "0" 1: Set the parity period data to "0"

beron	8E	[3]	W	0x0	Serial output changeover 0: TS serial data/clock 1: BER measurement serial data/clock
pkstop	8E	[2]	W	0x0	TS serial output clock setting for parity period 0: Issue clock during the parity period as well (204 bytes) 1: Stop clock during the parity period (188 bytes) * Does not function for TS parallel.
nuval	8E	[1]	W	0x0	Null packet period valid flag setting Data multiplexed null packets are out of scope. 0: Valid flag on 1: Valid flag off
valrev	8E	[0]	W	0x0	Valid polarity inversion 0: Data period "1," parity period "0" 1: Parity period "1," data period "1"
iits [15:8]	8F	[7:0]	W	0x00	Output TS_ID setting (Upper)
iits [7:0]	90	[7:0]	W	0x00	(Lower) When the specified TS_ID does not exist, the TS being sent in the first slot of the transmission frame is output.
anuval	A3	[7]	W	0x0	Valid flag setting for automatic/forced null packet replacement When nuval = "1," the valid flag for automatic and forced null packet replacement does not turn on. 0: Valid flag on 1: Valid flag off
cych[2:0]	A3	[6:4]	W	0x7	High-layer measurement cycle setting value In Slot Mode In Time Mode 0 384 packets 1 super frame 1 768 packets 2 super frames 2 1536 packets 4 super frames 3 3072 packets 8 super frames 4 6144 packets 16 super frames 5 12288 packets 32 super frames 6 24576 packets 64 super frames 7 49152 packets 128 super frames
asyncng	A3	[3]	W	0x0	TS packet error setting at demodulation pull-in setting Turns OFF the function that forcibly sets a TS packet (including null packet) error during the asynchronous period until demodulation pull-in completion. 0: Forcibly set error during asynchronous period 1: Do not forcibly set error during asynchronous period
cycl[2:0]	A3	[2:0]	W	0x7	Low-layer measurement cycle setting value In Slot Mode In Time Mode 0 384 packets 1 super frame 1 768 packets 2 super frames 2 1536 packets 4 super frames 3 3072 packets 8 super frames 4 6144 packets 16 super frames 5 12288 packets 32 super frames 6 24576 packets 64 super frames 7 49152 packets 128 super frames
rsckrev	A4	[7]	W	0x0	TS byte clock inversion Inverts the RSCKO clock polarity. 0: Normal, 1: Inversion Inversion

shch[2:0]	A4	[6:4]	W	0x0	Threshold value setting of automatic null packet replacement (null packet replacement stop) Threshold value for assessing "null packet replacement OFF" when error count increases 0 1/8 of cycle 1 1/16 of cycle 2 1/32 of cycle 3 1/64 of cycle 4 1/128 of cycle 5 1/256 of cycle 6 1/512 of cycle 7 Error counter = 1
shcl[2:0]	A4	[2:0]	W	0x0	Threshold value setting of automatic null packet replacement (null packet replacement start) Threshold value for assessing “null packet replacement ON” when error count increases Value Threshold value 0 1/8 of cycle 1 1/16 of cycle 2 1/32 of cycle 3 1/64 of cycle 4 1/128 of cycle 5 1/256 of cycle 6 1/512 of cycle 7 Error counter = 1
tschh	A5	[7]	W	0x0	Measurement cycle setting of number of error packets 0: Slot mode, 1: Time mode
corchh	A5	[6]	W	0x0	Error measurement mode setting 0: No. of error packets after RS decoding count mode 1: No. of error packets after Viterbi decoding count mode
jperst	A5	[0]	W	0x0	Forced resetting of high/low-layer error count 0: Do not reset. 1: Reset.
erval[2:0]	A6	[6:4]	W	0x0	Number of continuous error TS packets for RLOCK erval No. of Assessed Packets 0 1 (erval default value) 1 2 2 4 3 8 4 16 5 32 6 64 7 128
oponff	A6	[3]	W	0x0	High-layer forced null replacement ON 0: Do not replace with null. 1: Replace with null.
okval[2:0]	A6	[2:0]	W	0x4	Number of continuous error free TS packets for RLOCK okrval No. of assessed packets 0 1 1 2 2 4 3 8 4 16 (okval default value) 5 32 6 64 7 128
rlockh	C5	[1]	R	0xX	High-layer RLOCK monitor 0: RS decoding error, 1: No RS decoding error
rlockl	C5	[0]	R	0xX	Low-layer RLOCK monitor 0: RS decoding error, 1: No RS decoding error ("0" when layers do not exist)

nul_h	E8	[7]	R	0xX	High-layer automatic null replacement decision result monitor 0: Do not replace with null. 1: Replace with null.
nul_l	E8	[3]	R	0xX	Low-layer automatic null replacement decision result monitor 0: Do not replace with null. 1: Replace with null.
perrh [23:16]	EB	[7:0]	R	0xXX	High-layer error count monitor (Upper)
perrh [15:8]	EC	[7:0]	R	0xXX	(Middle)
perrh [7:0]	ED	[7:0]	R	0xXX	(Lower)
pecyh [15:8]	EE	[7:0]	R	0xXX	High-layer error count cycle monitor (Upper)
pecyh [7:0]	EF	[7:0]	R	0xXX	(Lower)
perrl [23:16]	F0	[7:0]	R	0xXX	Low-layer error count monitor (Upper)
perrl [15:8]	F1	[7:0]	R	0xXX	(Middle)
perrl [7:0]	F2	[7:0]	R	0xXX	(Lower)
pecyl [15:8]	F3	[7:0]	R	0xXX	Low-layer error count cycle monitor (Upper)
pecyl [7:0]	F4	[7:0]	R	0xXX	(Lower)

8.10 Monitor Output

The monitor registers provided in the TC90512 PSK demodulator, including the registers described thus far, are listed below.

8.10.1 TMCC Information Monitor Register

The TMCC information register allows you to monitor all transmitted TMCC information other than relative TS and slot information.

8.10.2 Constellation Monitor Register

The constellation can be read by the tsic register with the tston register="1."

8.10.3 Other Monitor Registers

1) The TS_ID number corresponding to the relative TS number "n" can be monitored by the tsid("n") register.

2) The total number of slots of TS to be output can be monitored by the acnt register. When the modulation QPSK and BPSK are included, the total number including dummy slots is output.

3) The modulation mode of the TS to be output can be monitored for each layer by the rateh and ratel registers, and the number of TS slots can be monitored for each layer by sloth and slotl. When the modulation QPSK and BPSK are included, the number of slots including dummy slots is output. With a single layer where layer modulation is not performed, the value is indicated in the high-layer register.

Name	Address (HEX)	Data	R/W	Initial Value	Description
tston	57	[7]	W	0x0	Constellation output ON 0: Output ON, 1: Output OFF
tsic[15:8]	B8	[7:0]	R	0xXX	Constellation I-axis data 2's complement format
tsic[7:0]	B9	[7:0]	R	0xXX	Constellation Q-axis data 2's complement format
crunlock	BA	[7]	R	0xX	Carrier asynchronous monitor Indicates the asynchronous state of the demodulation section. 0: Synchronized, 1: Not synchronized
agcmc [6:0]	BA	[6:0]	R	0xXX	AGC control volume monitor output 0: Minimum to 127: Maximum
afcfrq [7:0]	BB	[7:0]	R	0xXX	Carrier frequency error monitor Indicates the carrier frequency error. 2's complement expression -128 - 127
cnmc [15:8]	BC	[7:0]	R	0xXX	C/N monitor (Upper)
cnmc [7:0]	BD	[7:0]	R	0xXX	(Lower) Straight binary format. Indicates that the greater the value, the higher the noise level. (Phase noises are excluded.)
clkfrq [7:0]	BE	[7:0]	R	0xXX	Clock frequency error monitor 2's complement expression. Clock frequency error can be calculated using the following equation: Frequency error [ppm] = clkfrq x JFS[MHz]/MD[MHz] x 7.63 JFS (symbol rate) = 28.86[MHz]
inpnon	C3	[7]	R	0xX	Status register 1 flag inpnon Flag for monitoring the presence of input signals 0: Input signal level normal 1: Input signal level too low

unlock	C3	[6]	R	0xX	Status register 1 flag unlock 0: Synchronization normal 1: Out of frame synchronization and demodulation
crslip	C3	[5]	R	0xX	Status register 1 flag crslip 0: No carrier recovery cycle slip 1: Carrier recovery cycle slip
tmcerr	C3	[4]	R	0xX	Status register 1 flag tmcerr 0: No TMCC decoding error 1: TMCC decoding error
sdive	C3	[3]	R	0xX	sdive flag of status register 1 0: No TMCC site diversity switching 1: TMCC site diversity switching in progress
emgcy	C3	[2]	R	0xX	emgcy flag of status register 0 0: No TMCC emergency alarm broadcast start flag 1: TMCC emergency alarm broadcast start flag
tmcrev	C3	[1]	R	0xX	tmcrev flag of status register 1 0: No TMCC extension flag 1: TMCC extension flag
tmchg	C3	[0]	R	0xX	tmchg flag of status register 1 0: No change in TMCC change instruction flag 1: Change in TMCC change instruction flag
pm1d [4:0]	C5	[7:3]	R	0xXX	TMCC change instruction information monitor
acnt [5:0]	C6	[7:2]	R	0xXX	Total number of slots of output TS
uplink [3:0]	C7	[3:0]	R	0xX	TMCC uplink control information monitor
d_mode1 [3:0]	C8	[7:4]	R	0xX	Monitors TMCC transmission mode 1.
d_mode2 [3:0]	C8	[3:0]	R	0xX	Monitors TMCC transmission mode 2.
d_mode3 [3:0]	C9	[7:4]	R	0xX	Monitors TMCC transmission mode 3.
d_mode4 [3:0]	C9	[3:0]	R	0xX	Monitors TMCC transmission mode 4.
s_mode1 [5:0]	CA	[5:0]	R	0xXX	Monitor of number of slots assigned to TMCC transmission mode 1
s_mode2 [5:0]	CB	[5:0]	R	0xXX	Monitor of number of slots assigned to TMCC transmission mode 2
s_mode3 [5:0]	CC	[5:0]	R	0xXX	Monitor of number of slots assigned to TMCC transmission mode 3
s_mode4 [5:0]	CD	[5:0]	R	0xXX	Monitor of number of slots assigned to TMCC transmission mode 4
tsid0 [15:8]	CE	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 0 (Upper)
tsid0 [7:0]	CF	[7:0]	R	0xXX	(Lower)
tsid1 [15:8]	D0	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 1 (Upper)
tsid1 [7:0]	D1	[7:0]	R	0xXX	(Lower)
tsid2 [15:8]	D2	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 2
tsid2 [7:0]	D3	[7:0]	R	0xXX	
tsid3 [15:8]	D4	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 3
tsid3 [7:0]	D5	[7:0]	R	0xXX	
tsid4 [15:8]	D6	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 4
tsid4 [7:0]	D7	[7:0]	R	0xXX	

tsid5 [15:8]	D8	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 5
tsid5 [7:0]	D9	[7:0]	R	0xXX	
tsid6 [15:8]	DA	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 6
tsid6 [7:0]	DB	[7:0]	R	0xXX	
tsid7 [15:8]	DC	[7:0]	R	0xXX	Monitor of TS_ID corresponding to relative TS number 7
tsid7 [7:0]	DD	[7:0]	R	0xXX	
exfld [60:53]	DE	[7:0]	R	0xXX	TMCC extended area monitor (61 bits total) (Upper)
exfld [52:45]	DF	[7:0]	R	0xXX	
exfld [44:37]	E0	[7:0]	R	0xXX	
exfld [36:29]	E1	[7:0]	R	0xXX	
exfld [28:21]	E2	[7:0]	R	0xXX	
exfld [20:13]	E3	[7:0]	R	0xXX	
exfld [12:5]	E4	[7:0]	R	0xXX	
exfld [4:0]	E5	[7:3]	R	0xXX	(Lower)
tsido [15:8]	E6	[7:0]	R	0xXX	TS_ID number of output TS (Upper)
tsido [7:0]	E7	[7:0]	R	0xXX	(Lower)
rateh [2:0]	E8	[6:4]	R	0xX	Modulation mode of output TS (high layer) 111: 8PSK 110: QPSK R=7/8 101: QPSK R=5/6 100: QPSK R=3/4 011: QPSK R=2/3 010: QPSK R=1/2 001: BPSK 000: None
ratel [2:0]	E8	[2:0]	R	0xX	Modulation mode of output TS (low layer) 111: 8PSK 110: QPSK R=7/8 101: QPSK R=5/6 100: QPSK R=3/4 011: QPSK R=2/3 010: QPSK R=1/2 001: BPSK 000: None
sloth [5:0]	E9	[5:0]	R	0xXX	Number of slots of output TS (high layer)
slotl [5:0]	EA	[5:0]	R	0xXX	Number of slots of output TS (low layer)

8.11 I²C Through Mode

TC90512 is provided with the I²C through control pins JTNSCL and JTNSDA for setting the digital satellite tuner.
The I²C through mode is enabled by accessing register address "FEh." The enabled state is cleared at the stop condition after a series of data transfers has ended. (Refer to Section 5.1.)

Name	Address (HEX)	Data	R/W	Initial Value	Description
tnflg [7:0]	FE	[7:0]	W	0x00	Sets the address and subsequently the I2C bus through mode [7:1]: Tuner slave address [0]: Write to tuner at "0" Read from tuner at "1"

9. Digital Terrestrial (OFDM) Demodulation Functions

9.1 Reset

The OFDM demodulation circuit has the following two reset signals:
1) Demodulation reset (imsrst) that resets the demodulation synchronization sequence
2) Window search reset (iwsrst) that starts FFT window search

After these resets are set, the setting automatically returns to "0" after about 4μs. Thus, the resets do not need to be set to "0" to stop the reset process. (For system reset details, refer to Chapter 7.)

It is recommended that demodulation reset imsrst should be performed when channel tuning begins. Although TC90512 carries out synchronous pull-in automatically even if demodulation reset is not performed at channel tuning, it takes long time since the synchronous sequence is initialized after the out-of-synchronization state is detected.
Note that FFT window search reset is provided for tests, so it need not be used in normal operation.

Name	Address (HEX)	Data	R/W	Initial Value	Description
imsrst	01	[6]	W	0x0	Demodulation reset 0: Normal operation 1: Reset (automatically returns to normal operation)
iwsrst	01	[4]	W	0x0	FFT window search reset (for tests) 0: Normal operation 1: Reset (automatically returns to normal operation)

9.2 Operation Mode Setting

9.2.1 Switching between 13-Segment OFDM and 3/1-Segment OFDM

TC90512 can demodulate three segments consisting of one segment at the IF center frequency and the two neighboring to both ends of the center segment in addition to 13-segment OFDM signal demodulation. These modes can be switched by the recvmd register. To receive 13-segment OFDM signals, set recvmd="0." To receive 1- or 3-segment OFDM signals, set recvmd="2" or "3" accordingly.

9.2.2 Input Bandwidth at 3/1-Segment OFDM Demodulation

(1) Receiving a partial reception segment (1 segment) of digital terrestrial TV broadcast

TC90512 can receive a partial reception segment (1 segment) of digital terrestrial TV broadcast without setting the input signal band to the 1-segment narrow band. That is, when laysel="3h" is set without changing the 13-segment reception mode to other modes, only layer A is TS-output and layers B and C are all replaced with null packets. Note that the output clock rate is the same as for 13-segment demodulation.

(2) Reception of digital terrestrial sound broadcast

Digital terrestrial sound broadcast uses linked transmission (8 segments are linked for VHF7ch) without guard band to increase the frequency utilization efficiency of 3-segment OFDM signals. When 1- or 3-segment OFDM signals are received by TC90512, the input signal bandwidth need not agree with the bandwidth of the received signal if recvmd is set in accordance with the number of receive segments. For example, inputs in 3-segment bandwidth can be demodulated to 1-segment signals. Similarly, inputs in the entire bandwidth of 8-segment linked transmission signals can be demodulated to 1- or 3-segment signals. Note that the output TS clock rate is the same as for 13-segment demodulation even in 3/1-segment reception mode.

9.2.3 Switching between 3- and 1-Segment Reception Modes for Digital Terrestrial Sound Broadcast

To receive digital terrestrial sound broadcast, specify a sub-channel in steps of 1/7 MHz. Figure 9.1 shows the relationship between sub-channel numbers and segment numbers. Since the signal processing procedure differs with segments in demodulation of ISDB-T signals, specify the center segment of the received signal when the 3/1-segment reception mode is selected.

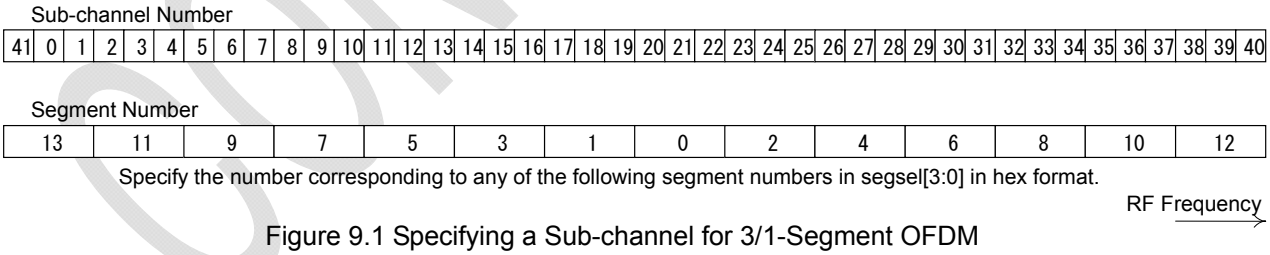


Figure 9.1 Specifying a Sub-channel for 3/1-Segment OFDM

Although 1-segment signals may be intermixed with 3-segment signals in digital terrestrial sound broadcast, TC90512 performs TMCC decision and can automatically demodulate signals according to the receivable segment type even if which segment type is transmitted. That is, 3-segment demodulation can be performed for input 3-segment signals, and 1-segment demodulation for input 1-segment signals. To enable this operation, set recvmdsel="1" together with the 3-segment reception mode (recvmd="3") in advance. If the TMCC parameter of the received signal is digital terrestrial sound (sysid=1) with 1-segment signals specified (part=0), the 1-segment reception mode is assumed automatically.

9.2.4 Digital Tuning Function of Digital Terrestrial Sound Broadcast

When the digital IF frequency conversion is changed in TC90512, the input IF center frequency is changed equivalently. With this digital tuning function, any segment can be demodulated without changing the IF signal frequency.
Digital tuning can be implemented by shifting the set value of the cpld_dt register in steps of segments (3/7 MHz). The cpld_dt equation is described in Section 9.8.1 "Frequency Conversion." Set the segment center frequency to be tuned to the IF frequency in the equation. To perform digital tuning for the segments with a 1-segment higher frequency, add 3/7 MHz to the IF frequency in the cpld_dt equation.
Table 9.1 summarizes the 3/1-segment OFDM demodulation functions and register settings of TC90512.

Table 9.1 3/1-Segment OFDM Demodulation Functions and Register Settings

		Segment signals to be demodulated		
Received signal	Input IF bandwidth	1-segment	3-segment	13-segment
Sound 1-segment	1-segment band (432 kHz)	recvmd="2"	—	—
Sound 3-segment (Partial reception segment + 2-segment)	3-segment band (1.3 MHz)	recvmd="2"	recvmd="3"	—
		recvmd="3," recvmdsel="1" (Note 2)		
Sound linked transmission (3- and 1-segment signals are mixed.)	8-segment band (3.5 MHz)(Note 1)	recvmd="2"	recvmd="3"	—
		recvmd="3," recvmdsel="1" (Note 2)		
TV layer transmission (Partial reception segment + 12-segment)	13-segment band (5.7 MHz)	recvmd="0," laysel="3h"	—	recvmd="0," laysel="0h"

Note 1) Example of VHF7ch (4 MHz) for digital terrestrial sound broadcast
Note 2) Demodulated in accordance with the number of input signal segments.

Name	Address (HEX)	Data	R/W	Initial Value	Description
recvmd [1:0]	02	[7:6]	W	0x0	Reception segment mode selection 0: TV reception (13-segment) 1: Test (disabled) 2: Sound reception (1-segment) 3: Sound reception (3-segment)
segsel [3:0]	02	[3:0]	W	0x0	Sets the center segment for sound reception 0 to 13
recvmdsel	EC	[3]	W	0x0	Reception mode switching for 3-segment reception 0: Fixed to 3-segment 1: Automatic switching between 1-segment and 3-segment
laysel [2:0]	71	[2:0]	W	0x0	Replaces the specified layer with a null packet. MSB [2]: Layer A 2nd MSB [1]: Layer B LSB [0]: Layer C 0: Do not replace with a null packet. 1: Replace with a null packet.

9.3 Standby Function

This function is used to stop (sleep status) the clock supply to the OFDM demodulation circuit except its I^2C control to reduce power consumption. This IC, however, can also monitor the emergency alarm broadcasting startup control signal transmitted by TMCC, while reducing power consumption, by performing modulation action (wakeup status) intermittently. The standby function can select any of the following three modes:

(1) Constant sleep status to reduce power consumption.
(2) Intermittent wakeup for monitoring the emergency alarm broadcasting startup control signal
(3) Intermittent wakeup for monitoring the emergency alarm broadcasting startup control signal, plus automatic resetting of sleep status while the startup control signal is detected.

In any case, the AD conversion circuit assumes the sleep status with power down when register slpadc="1," for lower power consumption.

9.3.1 Continuous Sleep

To select the first mode, set any value other than "0" to the sleep period set register watim and set "0" to the wakeup period set register wuptim.

9.3.2 Monitoring the Startup Control Signal (without Startup Control)

To select the second mode, set slpmd ="0" and set any value other than "0" to both of slptim and wuptim. Then the sleep status alternates with the wakeup status even when the startup control signal is detected.

Table 9.2 Setting the OFDM Demodulation Standby Operation (without Startup Control)

slpmd = "0"		Wakeup time	
		wuptim="0"	wuptim ≠ "0"
Sleep time	slptim="0"	Continuous wakeup	Continuous wakeup
	slptim ≠ "0"	Continuous sleep	Sleep and wakeup are repeated alternately.

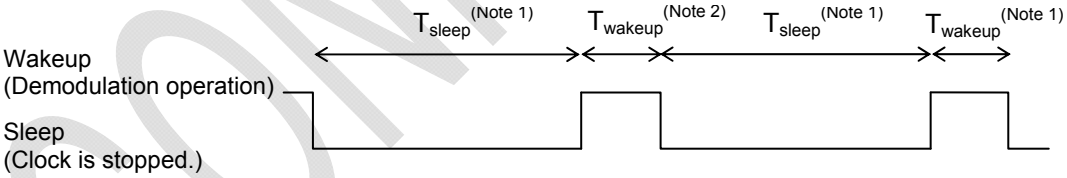


Fig. 9.2 Standby Operation without Startup Control

Note 1) Sleep period T_{sleep} is obtained by the following equation: For sleep, slptim can be set in the range of 1 to 7.

$$T_{sleep} = T_{wakeup} \times 2^{slptim} - 1$$

Note 2) Wakeup period T_{wakeup} is obtained by the following equation: For wakeup, wuptim can be set in the range of 1 to 15.

$$T_{wakeup} = wuptim \times 2^{25} \times (1/MD)$$

9.3.3 Monitoring the Startup Control Signal (with Startup Control)

To select the third mode, set slpmd ="1" and set any value other than "0" to both of slptim and wuptim. The wakeup status continues as long as the emergency alarm broadcasting startup control signal is detected, and the sleep status alternates with the wakeup status while that signal is not detected. The use of the sleep period set register and the wakeup period set register including the method of their setting are the same as those for a case where startup control is not performed.
It is possible to make modulation operation occur on the startup control signal detection emerg="1" only when each layer of the selected TS is judged free of error, by setting the emgmsk register ="1." For more information about error judgment, refer to Section 9.16.8.
The emergency alarm broadcast start flag emerg of received TMCC data can be output from the STSFLG0 pin by setting the stdisb register to "80h." In addition, the sleep/wakeup status can be output to the SLPEN pin as well as the slpen monitor register.(Refer to Section 9.4.)

Table 9.3 Setting the OFDM Demodulation Standby Operation (with Startup Control)

slpmd="1"		Wakeup time	
		wuptim="0"	wuptim ≠ "0"
Sleep time	slptim="0"	Continuous wakeup	Continuous wakeup
	slptim ≠ "0"	Continuous sleep	Sleep and wakeup are repeated alternately and wakeup is continued in the startup control signal detection period.

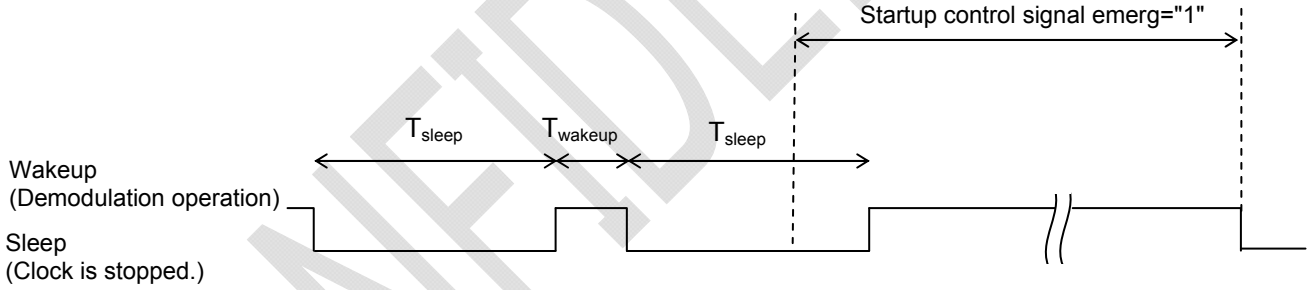


Fig. 9.3 Standby Operation with Startup Control

Name	Address (HEX)	Data	R/W	Initial Value	Description
slpmd	01	[3]	W	0x0	Set the operation when the startup control signal is detected. 0: Demodulation operation not restored by startup control signal emerg="1" 1: Demodulation operation restored by startup control signal emerg="1"
slplkmon	01	[2]	W	0x0	Set the wakeup conditions with startup control provided. 0: Always return to demodulation operation when the startup control signal is detected (emgcy="1"). 1: Always return to demodulation operation when the startup control signal is detected (emgcy="1"). (Enabled only when slpmd=1 and wuptim>0)
slpadc	03	[7]	W	0x0	Set ADC power down. 0: Do not power down the ADC for sleep. 1: Power down the ADC for sleep.

slptim [2:0]	03	[6:4]	W	0x0	Set the sleep time. 0: Demodulation operation without sleep (not dependent on slpmd and wuptim) 1-7: Sleep time ($(2^{slptim} - 1)$ x wakeup time) (no wakeup when wuptim=0)
wuptim [3:0]	03	[3:0]	W	0x0	Set the wakeup time. 0: No demodulation 1-15: Wakeup time (wuptim×2^{25}×MD cycle)

9.4 Input/Output Switching

9.4.1 Input Switching

(1) Differential input format and single-ended input format

ADC is either a differential or single-ended input. In either case, input is connected via the DC decoupling capacitor. In the case of single-ended input, input ADC to the ADI_AINP pin and AC-connect the ADQ_AINN pin to the analog GND. Note that register settings need not be changed when switching is made between differential and single ended.

(2) IF input and IQ baseband input

Input for OFDM demodulation can be made by IF signals in addition to baseband IQ signals. For IF signal input, refer to the setting method described in Section 6.5.

9.4.2 Output Signal Pin Switching

Designated output pins are grouped into System A, System B, System C and System D pins, as indicated below, allowing you to set each of the output signals.

Pin System	Pin Number									
	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
System A	H15	H14	D15	D14	E15	E14	F15	F12	G15	G14
System B	A9	B9	A10	B10	A11	B11	A12	B12	A13	B13
System C	A4	B4	A5	B5	A6	B6	A7	B7	A8	B8
System D	G1	G2	C1	C2	D1	D2	E1	E2	F1	F2

The signal that can be set are described below.

Signal System	Signal Name	Function
OFDM serial	SRCK	TS serial clock output
	SRDT	TS serial data output
	RSCKO	TS byte clock output
	SBYTE	TS synchronization byte flag output
	PBVAL	TS (packet) valid flag output
	RSEORF	RS decoding error (packet) flag output
	STSFLG1	Status register 1 output
	STSFLG0	Status register 0 output
	FLOCK	Frame synchronization flag output
	SLPEN	Sleep state flag output (“1”: Wakeup)
OFDM parallel	RLOCK	RS decoding error free flag
	RERR	RS decoding error flag
	RSOUT7	TS decoded data 7 output
	RSOUT6	TS decoded data 6 output
	RSOUT5	TS decoded data 5 output
	RSOUT4	TS decoded data 4 output
	RSOUT3	TS decoded data 3 output
	RSOUT2	TS decoded data 2 output
	RSOUT1	TS decoded data 1 output
	RSOUT0	TS decoded data 0 output

OFDM monitor	RLOCKA	RS decoding layer A error free flag
	RLOCKB	RS decoding layer B error free flag
	RLOCKC	RS decoding layer C error free flag
	RERRA	RS decoding layer A error flag
	RERRB	RS decoding layer B error flag
	RERRC	RS decoding layer C error flag
	STSFLG1	Status register 1 output
	STSFLG0	Status register 0 output
	HSEL1	Layer identification signal 1 output
	HSEL0	Layer identification signal 0

By default, the following pin assignments are made:

OFDM parallel signals are output to system A pins, and
OFDM serial signals are output to system B pins.

(System C pins are PSK serial signals, and system D pins are PSK parallel signals. and output settings for OFDM monitor signals are not made by default.)
These outputs can be changed by setting the pinsla, pinslb, pinslc, and pinsld registers. The outputs can also be changed by PSK registers when the pinsla, pinslb, pinslc, and pinsld registers are set to "3." (For the details of the PSK registers, refer to Section 8.3.)
The output enabled/disabled (High-Zor pull-down) initial state can be switched using the OEN pin. Output is enabled when OEN="0" and disabled when OEN="1." The OEN pin setting is incorporated in the IC when the SYRSTN pin changes from "0" to "1" (at power-on reset) and when isyrst is set. In addition, the enabled / "High-Z" or “pull-down” / fixed to "0" / fixed to "1" state can be individually set by setting the register corresponding to the output signal. In addition, the enabled / "High-Z" or "pull-down"/ fixed to "0" / fixed to "1" state can be individually set by setting the register corresponding to the output signal.
Furthermore, because register based enable control and polarity inversion control is performed against signals rather than pins, no change is required when pin assignments are changed by registers pinsla, pinslb, pinslc and pinsld.

9.4.3 Status Register

The contents of the status registers (addresses 80h and 81h) can be output to signals STSFLG1 and STSFLG0.

(1) Status register 1

This status register is output as the logical sum of the signals selected by the enable setting register (address 05h) from the 8 bits of status information described below. The same flag as for status register 1 is output for the JSTSFLG1 signal.

retryov: Synchronization pull-in sequence retry over flag
alarm: Alarm indicating that the AGC level is too high or low
tmunvld: Flag indicating that TMCC has not been obtained properly
mdunvld: Flag indicating that the recvmd setting is abnormal
fulock: Flag indicating that OFDM frame synchronization has not been obtained
vulock: Flag indicating that the Viterbi decoding circuit is abnormal (correction operation impossible)
rulock: Flag indicating that the TS decoding output contains errors more than specified
rseorf: Flag indicating that the TS packet output contains an error

The signals to be output are selected using the stdisa[7:0] register. The STSFLG output polarity can be switched using stinva[7:0]. The output format of the STSFLG1 signal can be selected so that output changes to "1" at the "0" to "1" or "1"to "0" change point using the stmda register. Note that the STSFLG1 signal is reset to "0" by resetting an arbitrary value to the stmda register.

(2) Status register 0

This status register is output as the logical sum of the signals selected by the enable setting register (address 06h) from the 5 bits of status information described below. The same flag as for status register 0 is output for the JSTSFLG0 signal.

emerg: Flag indicating that the emergency alarm broadcast start flag is set
tmcchg: Flag indicating that TMCC count-down is in progress.
cdunvld: Flag indicating mask period before and after TMCC count-down
slpen: Flag indicating the wakeup mode for standby operation.
STSFLG1: Flag indicating the result of status register 1 (only the status register selected by stdisa)

The signals to be output are selected using the stdisb[7:4] register. The STSFLG output polarity can be switched using stinvb[7:4]. The output format of the STSFLG0 signal can be selected so that output changes to "1" at the "0" to "1" or "1"to "0" change point using the stmdb register. Note that the STSFLG0 signal is reset to "0" by resetting an arbitrary value to the stmdb register.

9.4.4 Error Free Flag

The error free flag or error flag of output TS can be output to a pin.

RLOCK: RS decoding error free flag
RERR: RS decoding error flag

In addition, the flag for each layer shown below can be output to a pin as an OFDM monitor signal system.

RLOCKA/RLOCKB/RLOCKC: RS decoding error free flag of each layer
RERRA/RERRB/RERRC: RS decoding error flag of each layer

The output format of each flag can be selected so that output changes to "1" at the "0" to "1" or "1" to "0" change point using the rlmd register. Note that the each signal is reset to "0" by resetting an arbitrary value to the rlmd register.
For more information about each signal, refer to Section 9.15.8

9.4.5 Frame Synchronization Flag

A flag to indicate detection of OFDM frame synchronization of ISDB-T signal transmission can be output as an FLOCK signal.
The output format of frame synchronization flag output FLOCK can be selected so that output changes to "1" at the "0" to "1" or "1" to "0" change point using the flmd register. Note that the FLOCK signal is reset to "0" by resetting an arbitrary value to the flmd register.

9.4.6 Layer Identification Flag

The RLOCK and RERR signals can be switched to the layer identification signals HSEL1 and HSEL0 shown below by setting "1" to the hselout register. HSEL1 contains higher bits and HSEL0 contains lower bits to identify a layer and null for each packet as shown below:

Layer Identification Flag Output when the hselout register="1"

HSEL1 (RLOCK pin)	HSEL0 (RERR pin)	Identified layer
0	0	Layer A packet
0	1	Layer B packet
1	0	Layer C packet
1	1	Null packet

Name	Address (HEX)	Data	R/W	Initial Value	Description
stdisa [7:0]	05	[7:0]	W	0x00	STSFLG1 output setting Sets the validity of the status registers to be output to STSFLG1 for each bit. [7] retryov [6] alarm [5] tmunvld [4] mdunvld [3] fulock [2] vulock [1] rulock [0] rseorf 0: Disable, 1: Enable
stdisb [7:3]	06	[7:3]	W	0x0	STSFLG0 output setting Sets the validity of the status registers to be output to STSFLG0 for each bit. [7] emerg [6] tmcchg [5] cdunvld [4] slpen [3] STSFLG1 (only the status registers selected by stdisa) 0: Disable, 1: Enable
stinva [7:0]	07	[7:0]	W	0x0	STSFLG1 output polarity inversion Switches the polarity of the status registers output to STSFLG1 for each bit. Bit assignment is the same as for stdisa. 0: Normal, 1: Inverted
stinvb [7:3]	08	[7:3]	W	0x0	STSFLG0 output polarity inversion Switches the polarity of the status registers output to STSFLG0 for each bit. Bit assignment is the same as for stdisb. 0: Normal, 1: Inverted
stmda [1:0]	0C	[7:6]	W	0x0	STSFLG1 output mode setting Output mode of status registers output to STSFLG[1] 0: Normal (“1” when conditions occur) 1: "1" with change from 0 to 1 2: "1" with change from 1 to 0 3: "1" with change from 0 to 1 and 1 to 0 (Flag reset when other than 0 written)
stmdb [1:0]	0C	[5:4]	W	0x0	STSFLG0 output mode setting Output mode of status registers output to STSFLG[0] 0: Normal (“1” when conditions occur) 1: "1" with change from 0 to 1 2: "1" with change from 1 to 0 3: "1" with change from 0 to 1 and 1 to 0 (Flag reset when other than 0 written)
flmd [1:0]	0C	[3:2]	W	0x0	FLOCK output mode 0: Normal ("1" when conditions occur) 1: "1" with change from 0 to 1 2: "1" with change from 1 to 0 3: “1” with change from 0 to 1 and 1 to 0 (Flag reset at writing of value other than 0)

rlmd [1:0]	0C	[1:0]	W	0x0	RLOCK/RERR output mode 0: Normal ("1" when conditions occur) 1: "1" with change from 0 to 1 2: "1" with change from 1 to 0 3: "1" with change from 0 to 1 and 1 to 0 (Flag reset at writing of value other than 0)
pinsld [1:0]	0F	[7:6]	W	0x3	System D output pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal
pinslc [1:0]	0F	[5:4]	W	0x3	System C output pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal
pinslb [1:0]	0F	[3:2]	W	0x1	System B output pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal
pinsla [1:0]	0F	[1:0]	W	0x0	System A output pin output signal selection 0: Output OFDM parallel TS signal 1: Output OFDM serial TS signal 2: Output OFDM monitor signal 3: Output PSK signal
agccntioen [1:0]	1C	[7:6]	W	OEN	AGCCNTI signal output control 0 or OEN="0": Enable 1 or OEN="1": Disable (3-state output buffer: High-Z state, pull-down) 2: Fixed to "0" 3: Fixed to "1"
agccntroen [1:0]	1C	[5:4]	W	OEN	AGCCNTR signal output control 0 or OEN="0": Enable 1 or OEN="1": Disable (3-state output buffer: High-Z state, pull-down)2: Fixed to "0" 3: Fixed to "1"
stsflg1oen [1:0]	1C	[3:2]	W	OEN	STSFLG1 signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
stsflg0oen [1:0]	1C	[1:0]	W	OEN	STSFLG0 signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
rlockoen [1:0]	1D	[7:6]	W	OEN	RLOCK signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
rerroen [1:0]	1D	[5:4]	W	OEN	RERR signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
rsoutoen [1:0]	1D	[3:2]	W	OEN	RSOUT signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"

hselout	1D	[0]	W	0x0	Switching between RLOCK and RERR/HSEL 0: Output RLOCK and RERR 1: Output HSEL1 and HSEL0. HSEL[1:0]= 0: Layer A packet 1: Layer B packet 2: Layer C packet 3: Null packet (excluding transmission null packets)
flockoen [1:0]	1E	[7:6]	W	OEN	FLOCK signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
slpenoen [1:0]	1E	[5:4]	W	OEN	SLPEN signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
sroen [1:0]	1E	[3:2]	W	OEN	SRCK/SRDT signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
rsckooen [1:0]	1E	[1:0]	W	OEN	RSCKO signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
sbyteoen [1:0]	1F	[7:6]	W	OEN	SBYTE signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
pbvaloen [1:0]	1F	[5:4]	W	OEN	PBVAL signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"
rseorfoen [1:0]	1F	[3:2]	W	OEN	RSEORF signal output control 0 or OEN="0": Enable 1 or OEN="1": High-Z 2: Fixed to "0" 3: Fixed to "1"

* OEN: Determined by the OEN pin setting at power-on reset and at register-based isyrst reset.

9.5 Clock Setting

9.5.1 Clock Frequency Offset Correction

To set the ratio of the master clock frequency to the data frequency required for data resampling, the value (rounded down to nearest integer) calculated using the following equation is set in the hkfrq[15:0] register. When the standard frequency is used, the user need not set hkfrq because it is automatically set by XSEL1 and XSEL0. For details, refer to Section 6.5 and Chapter 10.

(1) 57 MHz IF mode (XT=25 MHz)

$$hkfrq = (XT \times 3 / FS - 1) \times 2^{16} \quad \text{(Equation 9-5-1)}$$

FS: Data frequency [MHz] = (65.015873)
XT: Reference clock frequency [MHz] (MD=3XT)

(2) 57 MHz IF mode (XT=20 MHz)

$$hkfrq = (XT \times 4 / FS - 1) \times 2^{16} \quad \text{(Equation 9-5-2)}$$

FS: Data frequency [MHz] = (65.015873)
XT: Reference clock frequency [MHz] (MD=4XT)

(3) 4 MHz IF mode and IQ baseband mode (XT=4 MHz)

$$hkfrq = (MD / FS - 1) \times 2^{16} \quad \text{(Equation 9-5-3)}$$

FS: Data frequency [MHz] = (65.015873)
MD: Master clock frequency [MHz]

hkfrq is a positive number. For calculation examples, refer to the next section.

9.5.2 Clock Frequency Control Range

With register hkncog[1:0], the clock frequency control range can be set. The absolute value $\Delta f/f$ in the range of frequency control range is calculated by the following equation:

$$|\Delta f / f| = (1 - (hkfrq + 2^{16}) / (hkfrq + 2^{(5-hkncog)} + 2^{16})) \times 10^6 \text{ [ppm]} \quad \text{(Equation 9-5-4)}$$

The frequency control clock that TC90512 can pull in falls in a range covering positive to negative values. A calculation example is shown below.

Example 1: 57 MHz IF mode (XT=25.400 MHz)
XSEL1 = 0
XSEL0 = 0
iexdiv = 0Bh (11) ····· Set automatically by XSEL1 and XSEL0.
ilpdiv = 21h (33) ····· Set automatically by XSEL1 and XSEL0.
MD = 76.200 MHz
hkfrq = 2C0Ah (11,274) ····· Set automatically by XSEL1 and XSEL0.
$\Delta f / f$ = ± 416ppm (hkncog = 0)
= ± 208ppm (hkncog = 1) ····· Initial Value
= ± 104ppm (hkncog = 2)
= ±52ppm (hkncog = 3)

Example 2: 57 MHz IF mode (XT=20.500 MHz)
XSEL1 = 0
XSEL0 = 1
iexdiv = 08h (8) ····· Set automatically by XSEL1 and XSEL0.
ilpdiv = 20h (32) ····· Set automatically by XSEL1 and XSEL0.

MD = 82.000 MHz
hkfrq = 42E0h (17,120) ····· Set automatically by XSEL1 and XSEL0.
Δf / f = ± 387 ppm (hkncog = 0)
= ±194ppm (hkncog = 1)·····Initial Value
= ± 97 ppm (hkncog = 2)
= ± 48 ppm (hkncog = 3)

Example 3: 4 MHz IF mode or IQ baseband mode (XT=4 MHz)
XSEL1 =1
XSEL0 = 0
iexdiv = 02 h (2)····· Set automatically by XSEL1 and XSEL0.
ilpdiv = 27h (39)····· Set automatically by XSEL1 and XSEL0.
MD = 78.000 MHz
hkfrq = 3320 h (13,088) ····· Set automatically by XSEL1 and XSEL0.
Δf / f = ± 406 ppm (hkncog = 0)
= ± 203 ppm (hkncog = 1) ····· Initial Value
= ± 101 ppm (hkncog = 2)
= ± 51 ppm (hkncog = 3)

If hkncog="1" (initial value) is set, a clock frequency deviation of about ±200 ppm can be pulled in. Note that the hkncog register is set with the upper limit value of the clock control loop filter. Since Δ f/f shown above is the value obtained by converting this upper limit value based on frequency drift, it does not always match the range where the clock frequency error is detectable. Specifically, if hkncog = "0," the clock frequency drift range that can be actually pulled in is smaller than the value shown above. Typically, hkncog ="1" is assumed and the corresponding Δf/f is regarded as the clock frequency drift pull-in range.

Name	Address (HEX)	Data	R/W	Initial Value	Description
ilpdiv [5:0]	11	[5:0]	W	XSEL	Clock division ratio (local side) setting Clock division ratio n=1 to 63
iexdiv [5:0]	12	[5:0]	W	XSEL	Clock division ratio (external reference) setting Clock division ratio n=1 to 63
hkfrq [15:8]	13	[7:0]	W	XSEL	Sampling clock frequency ratio setting 57 MHz IF/XT=25 MHz: hkfrq = (XT x 3 / FS-1) x 2^{16} 57 MHz IF/XT=20 MHz: hkfrq = (XT x 4 / FS-1) x 2^{16} 4 MHz IF/XT=4 MHz: hkfrq = (MD / FS-1) x 2^{16} IQ/XT=4 MHz: hkfrq = (MD / FS-1) x 2^{16} FS: Data frequency [MHz] = (65.015873) MD: Master clock frequency [MHz] XT: Reference clock frequency [MHz] * Set a value of 0x40 or greater.
hkfrq [7:0]	14	[7:0]	W	XSEL	
hkncog [1:0]	15	[7:6]	W	0x1	Clock frequency control range setting Δf / f =(1-(hkfrq + 2^{16})/(hkfrq + $2^{(5-hkncog)}$ + 2^{16})) x 10^6 [ppm] 0: x 1 (± 400 ppm) 1: x 1/2 (± 200 ppm) 2: x 1/4 (± 100 ppm) 3: x 1/8 (± 50 ppm)

* The registers with XSEL described in the "Initial value" column have the initial values specified by the settings of the XSEL1 and XSEL0 pins. For details, refer to Section 6.5 and Chapter 10.

9.6 Clock Recovery

TC90512 is provided with AFC and PLL for step-by-step loop gain switching, thereby allowing fast and steady pull-in operation. Since the loop gain is switched automatically by a sequencer, it need not be controlled from the outside.

9.6.1 Loop Gain Switching

The AFC loop uses double time constants. The narrow-band signal (1-segment or 3-segment reception) mode PLL switches the loop gain to one of three levels.

- The first loop gain of AFC is set to the clkg_h register.
- The second loop gain of AFC is set to the clkg_l register.
- The PLL loop gain in wide-band reception mode is set to the ckpldwg and ckpliwg registers.
- The first loop gain of PLL in narrow-band reception mode is set to the ckpld1g and ckpli1g registers.
- The second loop gain of PLL in narrow-band reception mode is set to the ckpld2g and ckpli2g registers.
- The third loop gain of PLL in narrow-band reception mode is set to the ckpld3g and ckpli3g registers.

Note that setting these loop gains individually should be avoided to ensure steady operation. They should be associated with each other for proper setting.

9.6.2 Frequency Error Monitor

The frequency error monitor function outputs the clock frequency error to register clkafc_dt. The frequency error is expressed by the following formula:

$$\Delta f / f = (1 - (hkfrq + 2^{16}) / (hkfrq + clkafc\_dt \times 2^{(-10-hkncog)} + 2^{16})) \times 10^{6}[ppm] \quad \text{(Equation 9-6-1)}$$

clkafc_dt is 16-bit data in 2's complement expression. A positive value indicates that the input signal frequency is higher than the TC90512 clock frequency. A negative value has a reverse meaning.

Name	Address (HEX)	Data	R/W	Initial Value	Description
clkg_h [1:0]	17	[7:6]	W	0x1	Gain setting for clock recovery AFC first pull-in Sets the loop gain for the clock AFC first pull-in operation. Increasing the setting value by 1 changes the gain by 1/2x. 0: Maximum gain to 3: Minimum gain
clkg_l [1:0]	17	[5:4]	W	0x3	Gain setting for clock recovery AFC second pull-in Sets the loop gain for the clock AFC second pull-in operation. Increasing the setting value by 1 changes the gain by 1/2x. 0: Maximum gain to 3: Minimum gain
ckpliwg [2:0]	18	[5:3]	W	0x6	Clock PLL integrating gain setting (wide-band reception mode) Sets the integrating gain of the PLL filter in wide-band reception mode. 0: Maximum gain β 1: Gain $\beta/2^4$ 2: Gain $\beta/2^6$ 3: Gain $\beta/2^8$ 4:: Gain $\beta/2^{10}$ 5: Gain $\beta/2^{12}$ 6: Gain $\beta/2^{14}$ 7: Minimum gain $\beta/2^{16}$

ckpli1g [2:0]	18	[2:0]	W	0x1	Clock PLL integrating gain setting (narrow-band reception mode) Sets the PLL filter integrating gain for the first pull-in operation in narrow-band reception mode. 0: Maximum gain β 1: Gain $\beta/2^4$ 2: Gain $\beta/2^6$ 3: Gain $\beta/2^8$ 4:: Gain $\beta/2^{10}$ 5: Gain $\beta/2^{12}$ 6: Gain $\beta/2^{14}$ 7: Minimum gain $\beta/2^{16}$
ckpli2g [2:0]	19	[5:3]	W	0x2	Clock PLL integrating gain setting (narrow-band reception mode) Sets the PLL filter integrating gain for the second pull-in operation in narrow-band reception mode. 0: Maximum gain β 1: Gain $\beta/2^4$ 2: Gain $\beta/2^6$ 3: Gain $\beta/2^8$ 4:: Gain $\beta/2^{10}$ 5: Gain $\beta/2^{12}$ 6: Gain $\beta/2^{14}$ 7: Minimum gain $\beta/2^{16}$
ckpli3g [2:0]	19	[2:0]	W	0x3	Clock PLL integrating gain setting (narrow-band reception mode) Sets the integrating gain of the PLL filter in narrow-band reception mode. 0: Maximum gain β 1: Gain $\beta/2^4$ 2: Gain $\beta/2^6$ 3: Gain $\beta/2^8$ 4:: Gain $\beta/2^{10}$ 5: Gain $\beta/2^{12}$ 6: Gain $\beta/2^{14}$ 7: Minimum gain $\beta/2^{16}$
ckpldwg [2:0]	1A	[5:3]	W	0x6	Clock PLL direct gain setting (wide-band reception mode) Sets the direct gain of the PLL filter in wide-band reception mode. 0: Maximum gain α 1: Gain $\alpha/2^2$ 2: Gain $\alpha/2^3$ 3: Gain $\alpha/2^4$ 4: Gain $\alpha/2^5$ 5: Gain $\alpha/2^6$ 6: Gain $\alpha/2^7$ 7: Minimum gain $\alpha/2^8$
ckpld1g [2:0]	1A	[2:0]	W	0x1	Clock PLL direct gain setting (narrow-band reception mode) Sets the PLL filter direct gain for the first pull-in operation in narrow-band reception mode. 0: Maximum gain α 1: Gain $\alpha/2^2$ 2: Gain $\alpha/2^3$ 3: Gain $\alpha/2^4$ 4: Gain $\alpha/2^5$ 5: Gain $\alpha/2^6$ 6: Gain $\alpha/2^7$ 7: Minimum gain $\alpha/2^8$

ckpld2g [2:0]	1B	[5:3]	W	0x2	Clock PLL direct gain setting (narrow-band reception mode) Sets the PLL filter direct gain for the second pull-in operation in narrow-band reception mode. 0: Maximum gain α 1: Gain $\alpha/2^2$ 2: Gain $\alpha 2^3$ 3: Gain $\alpha/2^4$ 4: Gain $\alpha/2^5$ 5: Gain $\alpha/2^6$ 6: Gain $\alpha/2^7$ 7: Minimum gain $\alpha/2^8$
ckpld3g [2:0]	1B	[2:0]	W	0x3	Clock PLL direct gain setting (narrow-band reception mode) Sets the direct gain of the PLL filter during normal operation in narrow-band reception mode. 0: Maximum gain α 1: Gain $\alpha/2^2$ 2: Gain $\alpha/2^3$ 3: Gain $\alpha/2^4$ 4: Gain $\alpha/2^5$ 5: Gain $\alpha/2^6$ 6: Gain $\alpha/2^7$ 7: Minimum gain $\alpha/2^8$
clkafc_dt [15:8]	86	[7:0]	R	0xXX	Carrier frequency error monitor output Indicates the clock frequency error. (2's complement format)
clkafc_dt [7:0]	87	[7:0]	R	0xXX	

9.7 AGC and Digital Filter

TC90512 outputs the AGC control signal for tuners. In addition, it can also output the RF AGC and IF AGC control signals. To output the RF AGC and IF AGC control signals, TC90512 carries out delay control (control to keep the RF AGC maximum gain up to the specified input level) for optimization of the tuner NF. Furthermore, by entering the tuner distortion signal (S_INFO signal) to TC90512, delay control can be controlled adaptively.
Moreover, in addition to the built-in digital filter to suppress adjacent channel interference, TC90512 has a built-in digital AGC to control the signal-level fluctuation caused by filtering.

9.7.1 Tuner AGC Control

TC90512 supports the "RF_AGC/IF_AGC switching control mode" and "IF_AGC control mode" as tuner AGC control schemes.
The AGC control signals are output from the AGCCNTR and AGCCNTI pins. As initial settings, the "0" period increases if the gain error is positive (the input level is higher than the reference level) and the "1" period increases if the gain error is negative (the input level is lower than the reference level). This polarity can be inverted by setting the rfagc_inv and ifagc_inv registers to "1."

(1) RF_AGC/IF_AGC switching control mode

The RF_AGC/IF_AGC switching control mode is set by setting the rfif register to "0."
In this mode, the RF_AGC and IF_AGC control outputs are used to keep the input signal level of the demodulation IC constant. This AGC works as a delayed AGC that switches between the RF_AGC and IF_AGC, depending on the RF input signal level. The switching level of the RF_AGC and IF_AGC is set by the delay point (RF/IF switching point) setting register delayp. As the delay point, set an optimum tradeoff value between the NF and distortion of the tuner in straight binary format. (Refer to Fig. 9.4.)
The initial value of the RF_AGC control output is set in the rf_max register, and the initial value of the IF_AGC control output is set in the delayp register. Both registers are initialized at the time of demodulation reset.

(2) IF_AGC control mode

The IF_AGC control mode is set by setting the rfif register to "1."
In IF_AGC control mode, which is provided for RF_AGC control at the tuner, only IF_AGC control output is produced. The RF_AGC control output of TC90512 is fixed to "0" and the delayp register functions to provide only the IF_AGC lower limit.
The initial value of the AGC control output in IF_AGC control mode is set in the ifmgc register that is initialized at the time of demodulation reset. Note, however, that if a value smaller than the delayp setting, the AGC is controlled by the lower limit set in delayp.

(3) Setting the delay point (RF/IF switching point)

The delay point is the RF_AGC and IF_AGC switching point in RF_AGC/IF_AGC switching control mode. When the full range of IF_AGC control output (AGCCNTI output pin) is expressed in 8-bit straight binary format as the delay point automatic control initial value, the value of the target IF_AGC control level is set to the delayp register.
Note that the setting of the delayp register when rfif = "1" functions as the lower limit value of IF_AGC. If a value smaller than ifagc_dt is set to delayp after demodulation reset, the AGC operation point gets smaller than the IF_AGC lower limit value, thus breaking the control operation down.
Do not use the rfif setting, but be sure to carry out demodulation reset after setting the delayp register.

(4) AGC control range limiter function

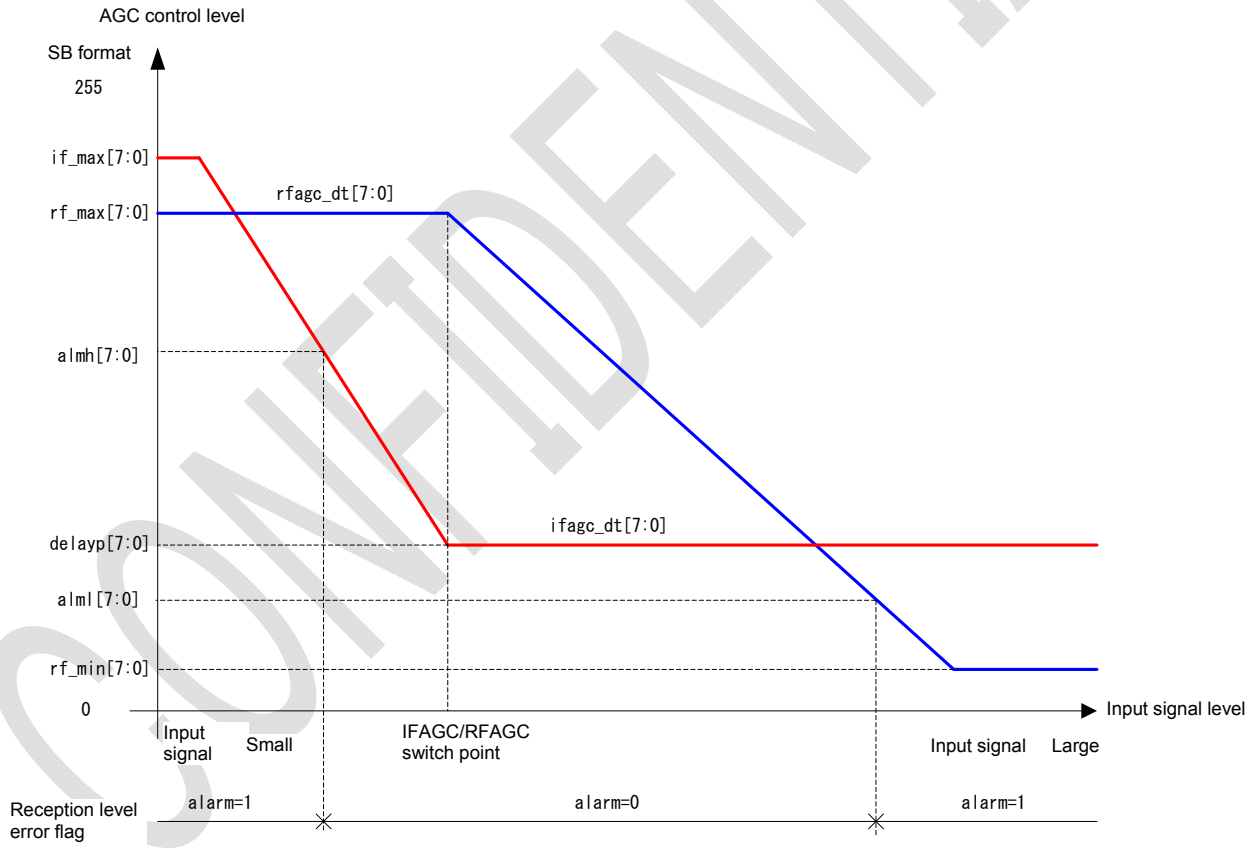
The AGC control range limiter function allows you to set the AGC control range upper limit (the limit value when the input signal level is low) and lower limit (the limit value when the input signal level is high). The RF_AGC control range upper limit is set in the rf_max register, and the lower limit is set in the rf_min register. The IF_AGC control range upper limit is set in the if_max register, and the lower limit is set in the delayp register.

(5) Reception level alarm function

The reception level alarm function detects reception level errors of the RF input signal (excessively high or excessively low input levels) and outputs "1" to the "alarm" reception level error flag register. The judgment level for reception level errors can be arbitrarily set to almh and alml.
In RF_AGC/IF_AGC switching control mode, the judgment threshold and IF_AGC control level are compared if the input is too low, and the judgment threshold and RF_AGC control level are compared if the input is too high.
In IF_AGC control mode, the judgment threshold is compared with the IF_AGC control level if the input is too low or too high. Note, however, that RF input cannot be assessed as excessively high when RF_AGC is performed externally.

(6) AGC control level monitor

The AGC control level monitor outputs the IF_AGC control volume (IF_AGC output) to the ifagc_dt register. In addition, the monitor also outputs the RF_AGC control volume (RF_AGC output) to the rfagc_dt register. Since both registers hold values in pulse format, suppress the harmonics components by using an external LPF.



Illustrative Diagram of AGC Control Operation (RFAGC/IFAGC Switch Control Mode)

Fig. 9.4 AGC Operation Illustrative Chart

(7) Correcting AGC control characteristics

When an AGC amplifier with nonlinear AGC control sensitivity is used, the AGC loop gain sometimes does not become constant, making it difficult to set a loop response even if the AGC error detection sensitivity of the demodulation IC is constant. TC90512 can switch gains in such a way that the nonlinear AGC control sensitivity can be corrected approximately.
As shown in the figure, TC90512 can switch two gains (ifagcg and ifagcg x ifsch, or rfagcg and rfagcg x rfsch) using ifthd or rfthd as change points for IF and RF, respectively. If these gains approximate the nonlinear characteristics of AGC control sensitivity, the loop gain as a total gain can be virtually set to a constant value.
The "ifthd" (or "rfthd") gain switching point setting register sets the full range of AGC control signals based on 16 levels. The control gains below the switching points are ifagcg and rfagcg, respectively. Those above the switching points are ifagcg x ifsch and rfagcg x rfsch, respectively. The ifsch and rfsch registers can be set at four levels (x8, x4 , x2, and x1).

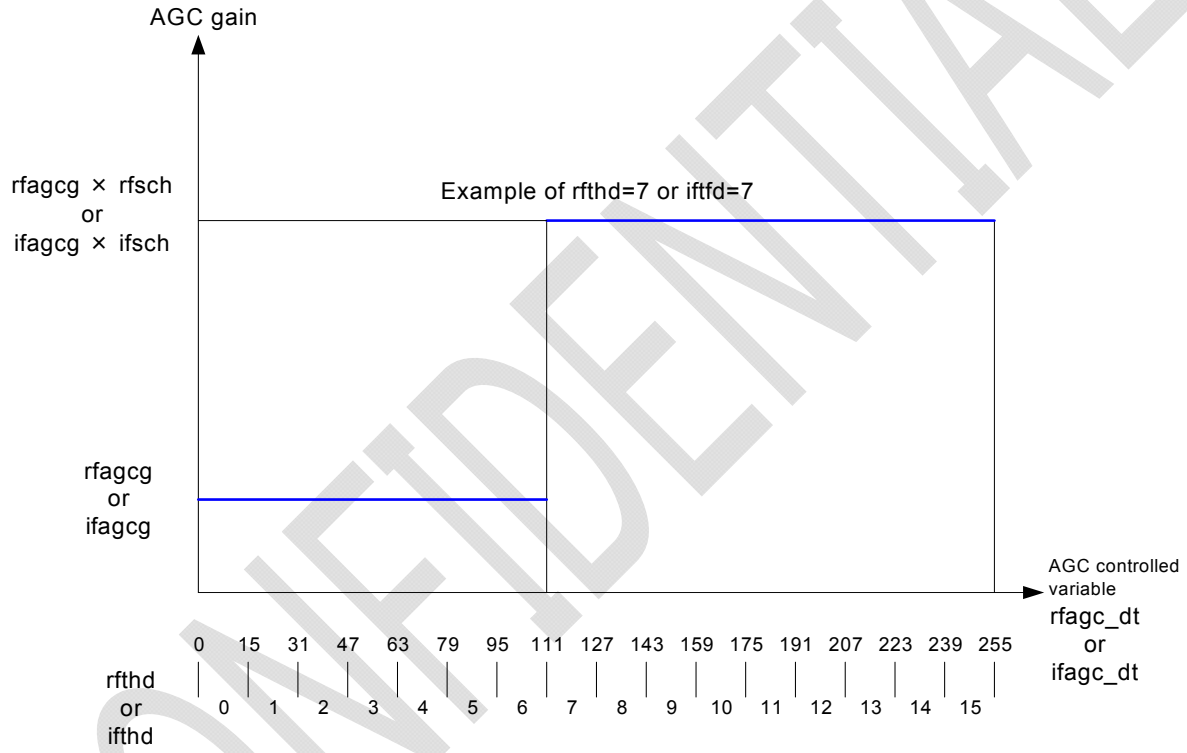


Figure 9.5 Correcting the AGC Control Characteristics

(8) AGC control at standby operation

The pin status of AGCCNTI and AGCCNTR is held at “0” in the sleep status of the standby operation. Note that, however, when the output of the ifagc_inv and rfagc_inv registers is polarity-inverted, the output in the sleep status is also polarity-inverted.

9.7.2 AGC Passthrough Function

When the agcthr register="1," the signals input to the AGCI pin can be through-output to the AGCCNTI pin. This is a useful method when the AGC control output of TC90512 is replaced by any other digital AGC control signal. (No analog AGC signals can be input.)

9.7.3 Digital Filter

TC90512 has a built-in digital filter that suppresses out-of-band unnecessary components including adjacent channel interferences. TC90512 supports multiple IF frequencies and reference clock frequency, enabling selection of digital filter characteristics in accordance with these settings. Selection from the following four types of filters is possible by the lpfsl register.
Note that lpfsl need not be set for normal operation except for XT=27 MHz mode because it is set automatically by the XSEL1 and XSEL0 pins. However, when the master clock frequency is different from standard frequencies, set lpfsl in accordance with the master clock frequency.

Table 9.4 Factor Switching of Adjacent Channel Interference Suppressing Digital Filter

lpfsl	Operation Mode	Master Clock Frequency [MHz]
0	For 4 MHz IF and IQ operation	78 MHz
1	For operation in 44 MHz IF (XT=19 MHz) mode(Note)	77.208 - 79.296
2	For operation in 57 MHz IF (XT=20 MHz) mode	81.868 - 83.000
3	For operation in 57 MHz IF (XT=25 MHz) mode	76.157 - 78.333

(Note) When the filter is used for frequencies such as 44 MHz IF, set the registers individually.

9.7.4 Digital AGC

TC90512 has a built-in digital AGC. The operation status of a digital AGC (automatically set gain) can be read from the dagc_dt register. This register saves data in 2's complement format. A positive value is a gain greater than 0 and a negative value is a gain smaller than 0. (In normal state in which the digital AGC gain is 1, "00h" is set in dagc_dt.)

Name	Address (HEX)	Data	R/W	Initial Value	Description
delayp [7:0]	20	[7:0]	R/W	0x00	Delay point (RF/IF switching) setting Sets the IF_AGC control level in SB format.
rf_max [7:0]	21	[7:0]	W	0xFF	RF_AGC maximum clip level setting Sets the RF_AGC limit value for a low level in SB format. FF: Maximum to 00: Minimum
rfif	22	[7]	W	0x1	AGC control method switching Switches the AGC control operating mode. 0: RF_AGC/IF_AGC switching control mode 1: IF_AGC control mode
agcthr	22	[4]	W	0x0	AGC passthrough ON/OFF switching 0: OFF, 1: ON
agdacnt [1:0]	22	[3:2]	W	0x0	IF/RF_AGC 1-bit DAC highest frequency rate limit setting Reduces the switching frequency. 0: 1 (no limitation) 1: 1/2 2: 1/4 3: 1/8
agdack [1:0]	22	[1:0]	W	0x0	IF/RF_AGC 1bit DAC operation clock setting 0: 1 to 32 MHz 2 to 32 MHz 3 to 8 MHz 4MHz
ifagcg1 [2:0]	23	[7:5]	W	0x2	IF_AGC loop gain setting (pull-in) 0: Maximum gain to 7: Minimum gain
ifagcg2 [2:0]	23	[4:2]	W	0x3	IF_AGC loop gain setting (steady condition) 0: Maximum gain to 7: Minimum gain
ifagc_inv	23	[1]	W	0x0	IF_AGC control AGCCNTI output polarity inversion Inverts the IF_AGC control signal polarity of AGCCNTI pin output. 0: If the input level is high, AGCCNTI output L period > H period If the input level is low, AGCCNTI output L period < H period 1: If the input level is high, AGCCNTI output H period > L period If the input level is low, AGCCNTI output H period < L period

ifmgcon	23	[0]	W	0x0	IF_AGC gain control manual setting selection Switches AGC and MGC operation. 0: Automatic control (AGC), 1: Manual setting (MGC)
rfagcg1 [2:0]	24	[7:5]	W	0x2	RF_AGC loop gain setting (pull-in) 0: Maximum gain to 7: Minimum gain
rfagcg2 [2:0]	24	[4:2]	W	0x3	RF_AGC loop gain setting 0: Maximum gain to 7: Minimum gain
rfagc_inv	24	[1]	W	0x0	RF_AGC control AGCCNTR output polarity inversion Inverts the RF_AGC control signal polarity of AGCCNTI pin output. 0: If the input level is high, AGCCNTR output L period > H period If the input level is low, AGCCNTR output L period < H period 1: If the input level is high, AGCCNTR output H period > L period If the input level is low, AGCCNTR output H period < L period
rfmgcon	24	[0]	W	0x0	RF_AGC gain control manual setting selection Switches AGC and MGC operation. 0: Automatic control (AGC), 1: Manual setting (MGC)
ifmgc [7:0]	25	[7:0]	W	0x00	IF gain manual setting Sets the IFMGC level output from the AGCCNTI pin in SB format when ifmgcon = 1. FF: Maximum to 00: Minimum
rfmgc [7:0]	26	[7:0]	W	0x00	RF gain manual setting Sets the RFMGC level output from the AGCCNTR pin in SB format when rfmgcon = 1. FF: Maximum to 00: Minimum
ifthd [3:0]	28	[3:0]	W	0x0	IF_AGC gain switching level setting Sets the level in SB format. F: Maximum to 0: Minimum
rfthd [3:0]	2B	[3:0]	W	0x0	RF_AGC gain switching level setting Sets the level in SB format. F: Maximum to 0: Minimum
almh [7:0]	2C	[7:0]	W	0xFF	Alarm level setting (low) Sets the alarm decision level for a low input level. Sets the alarm level ifagc_dt in SB format.
alml [7:0]	2D	[7:0]	W	0x00	Alarm level setting (high) Sets the alarm decision level for a high input level. Sets the alarm level rfagc_dt in SB format in RF/IF switching control mode.
if_max [7:0]	2E	[7:0]	W	0xFF	IF_AGC upper limit setting Sets the IF_AGC limit value in SB format for a low input level in SB format. FF: Maximum to 00: Minimum
rf_min [7:0]	2F	[7:0]	W	0x00	RF_AGC lower limit setting Sets the RF_AGC limit value in SB format for a high input level in SB format. FF: Maximum to 00: Minimum
lpfsl [1:0]	34	[5:4]	W	XSEL	Digital filter factor switching 0: For OFDM single operation at low IF 1: 44 MHz direct IF (for 19 MHz operation) 2: 57 MHz direct IF (for 20 MHz operation) 3: 57 MHz direct IF (for 25 MHz operation)
ifsch [1:0]	34	[3:2]	W	0x3	IF_AGC gain correction setting Sets the gain when the level is greater than the level set in ifthd. 0: 8 times, 1: 4 times, 2: 2 times, 3: 1 time
rfsch [1:0]	34	[1:0]	W	0x3	RF_AGC gain correction setting Sets the gain when the level is greater than the level set in rfthd. 0: 8 times, 1: 4 times, 2: 2 times, 3: 1 time

* SB: Straight binary Straight binary

9.7.5 AGC Adaptive Control by S_INFO

TC90512 is capable of controlling the AGC using the S_INFO pin input that is the distortion detection output of the tuner in the RF_AGC/IF_AGC switching control mode. (Use a signal that turns to "1" when the amount of distortion exceeds the allowable level as the distortion sense output of the tuner. A signal whose level is judged before IF_AGC would be appropriate.)
When the register sifon="1," the adaptive control function of the AGC that uses S_INFO works. The IF_AGC level is raised or dropped by the S_INFO signal, thus controlling the interlocking RF_AGC. To be specific, the IF_AGC gain is increased when the S_INFO signal indicates existence of some distortion so that the RF_AGC gain will be decreased. On the other hand, the IF_AGC gain is decreased when the S_INFO signal indicates existence of no distortion so that the RF_AGC gain will be increased.
The step width of the AGC adaptive control is set by the dpstep register, the control time constant is set by the dp_sft register, and the control interval is set by the dpcttim register. The control polarity of the S_INFO signal to be input can be inverted by the sifinv register. In addition, the upper limit of the control range can be set by the dplmth register, and its lower limit can be set by the dplmtl register. The control interval based on the S_INFO signal is set by register dpcttim. (The control interval is determined by dpcttim x 27.5 ms.)
Some registers may contain settings different from those in ordinary cases in the AGC control that uses the S_INFO signal as sifon="1." See the following tables:

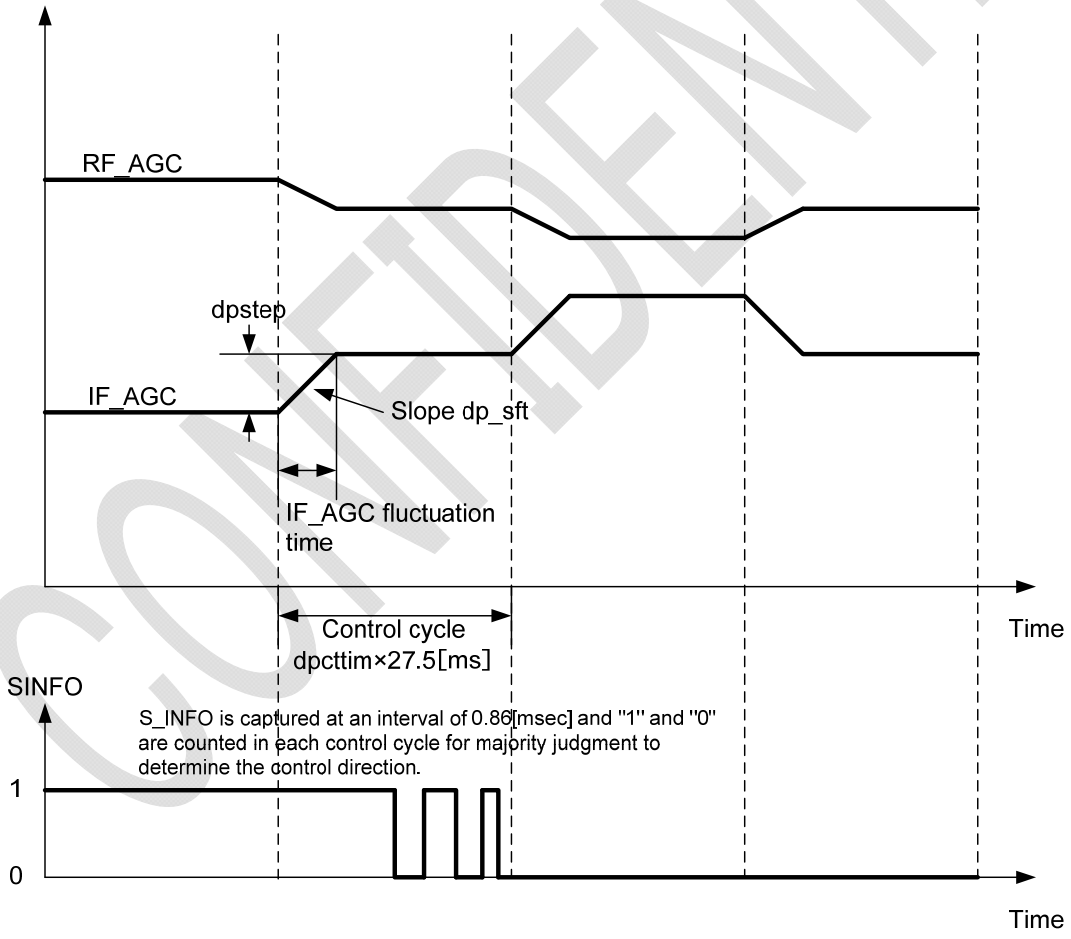


Figure 9.6 S_INFO Control

Name	Address (HEX)	Data	R/W	Initial Value	Description **(when sifon="1")**
delayp [7:0]	20	[7:0]	R/W	0x00	Initial value setting for S_INFO control Sets the initial value for S_INFO control (IF_AGC control level) in SB format.
sifon	22	[6]	W	0x0	ON/OFF switching of adaptive AGC control by S_INFO 0: OFF 1: ON
sifinv	22	[5]	W	0x0	S_INFO signal control polarity inversion 0: Normal, 1: Inversion
dpstep [7:0]	27	[7:0]	W	0x0C	S_INFO control step width setting 2's complement expression (starting from the step that lowers the RF gain when it is negative) Equivalent to IF_AGC full range/1024 at 1LSB
dp_sft [2:0]	28	[7:5]	W	0x3	S_INFO control time constant setting Time required for IF_AGC to change by 1/1024 of the full range 0: 165 ms 1: 82.5 ms 2: 41.2 ms 3: 20.6 ms 4: 10.3 ms 5: 5.1 ms 6: 2.5 ms 7: Disabled
dplmth [7:0]	29	[7:0]	W	0x6B	S_INFO signal control range higher limit value setting Sets the value in SB format. FF: Maximum to 00: Minimum
dplmtl [7:0]	2A	[7:0]	W	0x40	S_INFO signal control range lower limit value setting Sets the value in SB format. FF: Maximum to 00: Minimum
dpcttim [3:0]	2B	[7:4]	W	0x4	Control time interval setting for S_INFO control Set value x 27.5[ms]

* SB: Straight binary

9.8 Carrier Recovery

9.8.1 Frequency Conversion

The frequency of IF complex signals is converted to that of base-band complex signals. The offset frequency setting for frequency conversion is set by register cpld_dt.

(1) 57 MHz IF mode (XT=25 MHz)

$$cpld\_dt = (IF\ frequency\ [MHz] - XT \times 2) \times 10^6 \times (FS / MD) \times (3/4) / 992 \quad \text{(Equation 9-8-1)}$$

FS: Data frequency [MHz] = (65.015873)
MD: Master clock frequency [MHz]
XT: Reference clock frequency [MHz]

(2) 57 MHz IF mode (XT=20 MHz)

$$cpld\_dt = (XT \times 3 - IF\ frequency\ [MHz]) \times 10^6 \times (FS / MD) / 992 \quad \text{(Equation 9-8-2)}$$

FS: Data frequency [MHz] = (65.015873)
MD: Master clock frequency [MHz]
XT: Reference clock frequency [MHz]

(3) 4 MHz IF mode (XT=4 MHz)

$$cpld\_dt = (IF\ frequency\ [MHz]) \times 10^6 \times (FS / MD) / 992 \quad \text{(Equation 9-8-3)}$$

FS: Data frequency [MHz] = (65.015873)
MD: Master clock frequency [MHz]

(4) IQ baseband mode (XT=4 MHz)

$$cpld\_dt = (baseband\ center\ frequency[MHz]) \times 10^6 \times (FS / MD) / 992 \quad \text{(Equation 9-8-4)}$$

FS: Data frequency [MHz] = (65.015873)
MD: Master clock frequency [MHz]

When, for example, IF frequency=57.000 MHz and XT=25.400 MHz in 57 MHz IF (XT=25 MHz) mode, MD=76.2 MHz and cpld_dt is as follows:

$$cpld\_dt = (57.000 - 24.500 \times 2) \times 10^6 \times (65.015873 / 76.200) \times (3/4) / 992$$
$$= 4000\ (DEC)$$
$$= 0FA0\ (HEX)$$

The cpld_dt register need not be set for normal operation because it is set automatically by the XSEL1 and XSEL0 pins. For details, refer to Section 6.5 and Chapter 10.
Furthermore, the frequency spectrum polarity of signal processing needs to be considered in accordance with IF signal input. Demodulation is properly performed when the IF frequency spectrum polarity after AD conversion and the RF frequency spectrum polarity are the same, by default. For example, because the frequency spectrum polarity at 4 MHz Low IF is generally the same as that of RF, there is no need for polarity inversion. With the 57 MHz direct IF, if the reference clock frequency XT = 20.5 MHz, polarity inversion is not required since the ADC based frequency conversion is the same as the upper local oscillator frequency conversion. But if XT = 25.4 MHz, polarity inversion is required since the frequency conversion is equivalent to the lower local oscillator frequency conversion. Frequency spectrum polarity inversion is set by the f_inv register. Note, however, that the spectrum polarity inversion need not be set for normal operation because it is set automatically by the XSEL1 and XSEL0 pins.

9.8.2 Frequency Pull-in Range

The carrier frequency pull-in range is ±250 kHz or higher in 13-segment reception mode. On the other hand, the carrier frequency pull-in range is ±200 MHz in 1-segment or 3-segment reception mode. When the "recvmd" reception segment mode selection register is set, the frequency pull-in range is automatically switched.
In 1-segment reception or 3-segment reception mode, the frequency pull-in range can be switched to ±200 kHz or ±62 kHz by the sbchlmt register. This can be utilized in cases such as when the frequency pull-in range is too narrow at the time of digital terrestrial sound broadcast sub-channel tuning and the adjacent sub-channel gets pulled in.

9.8.3 Carrier AFC Loop Gain Correction Setting

The carrier AFC loop gain correction setting corrects the control sensitivity of the value control oscillator used in the carrier AFC pull-in operation in accordance with the master clock frequency. The correction value is set to the affrq register.

(1) 57 MHz IF mode (XT=25 MHz)

affrq = (1 - (FS / MD) x (3/4)) x 1024 (Equation 9-8-5)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

(2) 57 MHz IF mode (XT=20 MHz)

affrq = (1 - FS / MD) x 1024 (Equation 9-8-6)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

(3) 4 MHz IF mode (XT=4 MHz)

affrq = (1 - FS / MD) x 1024 (Equation 9-8-7)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

(4) IQ baseband mode (XT=4 MHz)

affrq = (1 - FS / MD) x 1024 (Equation 9-8-8)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

When, for example, IF frequency=57.000 MHz and XT=25.400 MHz in 57 MHz IF(XT=25 MHz) mode, MD=76.2 MHz and affrq is as follows:

affrq = ((1 - FS / MD) x (3/4)) x 1024
= 368 (DEC)
= 170 (HEX)

The affrq register need not be set for normal operation because it is set automatically by the XSEL1 and XSEL0 pins. For details, refer to Section 6.5 and Chapter 10.

9.8.4 Loop Gain Switching

The carrier frequency pull-in operation uses coarse synchronization and fine synchronization. For each, the time constant and loop filter gain can be set. Fine synchronization uses so-called double time constants, allowing you to set the gains for pull-in operation and steady operation. For switching between the double time constants a synchronization sequence timer is used.
The gain at the time of fine synchronization pull-in is set in the carg_h register. The gain at the time of fine synchronization steady operation is set in the carg_l register.

9.8.5 Carrier Frequency Error Monitor

The carrier frequency error monitor outputs the carrier frequency error to the carafc_dt register. The carrier frequency error is expressed by the following formulas:

(1) 57 MHz IF mode (XT=25 MHz)

Carrier frequency error = carafc_dt x 7.75 x (MD/FS) x (4/3) [Hz] (Equation 9-8-9)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

(2) 57 MHz IF mode (XT=20 MHz)

Carrier frequency error = carafc_dt x 7.75 x (MD/FS) [Hz] (Equation 9-8-10)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

(3) 4 MHz IF mode (XT=4 MHz)

Carrier frequency error = carafc_dt x 7.75 x (MD/FS) [Hz] (Equation 9-8-11)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

(4) IQ baseband mode (XT=4 MHz)

Carrier frequency error = carafc_dt x 7.75 x (MD/FS) [Hz] (Equation 9-8-12)
FS: Data frequency (=65.015873 MHz)
MD: Master clock frequency

Furthermore, when the IF input frequency polarity is inverted due to the relationship with the tuner local oscillator, the positive/negative sign of the carrier frequency error is also inverted.

Name	Address (HEX)	Data	R/W	Initial Value	Description
carg_h [1:0]	30	[7:6]	W	0x0	Carrier AFC loop gain 1 setting Selects the gain of carrier AFC for pull-in operation. Increasing the setting value by 1 changes the gain by 1/2x. 0: Maximum gain to 3: Minimum gain
carg_l [1:0]	30	[5:4]	W	0x2	Carrier AFC loop gain 2 setting Selects the gain of carrier AFC for steady operation. Increasing the setting value by 1 changes the gain by 1/2x. 0: Maximum gain to 3: Minimum gain
f_inv	30	[3]	W	XSEL	Digital IF frequency inversion Selects the frequency for converting the 2nd_IF signal into the base band signal. 0:Digital IF frequency polarity not inverted 1:Digital IF frequency polarity inverted
sbchlmt	30	[2]	W	0x0	Pull-in range at 3/1-segment reception Selects the frequency pull-in range at 3/1-segment reception. 0: ±200 kHz 1: ±62 kHz

cpld_dt [13:8]	31	[5:0]	W	XSEL	Carrier frequency offset value setting 57 MHz IF/XT25 MHz mode: cpld_dt = (IF - XT x 2) x 10^6 x (FS/MD) x (3/4) / 992 57 MHz IF/XT20 MHz mode: cpld_dt = (XT x 3 - IF) x 10^6 x (FS/MD) / 992 4 MHz IF mode: cpld_dt = (IF) x 10^6 x (FS/MD) / 992 IQ baseband mode: cpld_dt = (IF) x 10^6 x (FS/MD) / 992 FS: Data frequency [MHz] = (65.015873) MD: Master clock frequency [MHz] XT: Reference clock frequency [MHz] IF: IF frequency [MHz]
cpld_dt [7:0]	32	[7:0]	W	XSEL	
affrq [8]	38	[0]	W	XSEL	Carrier frequency correction factor 57 MHz IF/XT25 MHz mode: affrq = (1 - (FS/MD) x (3/4)) x 1024 57 MHz IF/XT20 MHz mode: affrq = (1 - FS/MD) x 1024 4 MHz IF mode: affrq = (1 - FS/MD) x 1024 IQ baseband mode: affrq = (1 - FS/MD) x 1024 FS: Data frequency [MHz] = (65.015873) MD: Master clock frequency [MHz]
affrq [7:0]	39	[7:0]	W	XSEL	
carafc_dt [15:8]	84	[7:0]	R	0xXX	Carrier frequency error monitor output Indicates the carrier frequency error. (2's complement format) When the receiver frequency is high, a negative (-) frequency error is output. When the receiver frequency is low, a positive (+) frequency error is output.
carafc_dt [7:0]	85	[7:0]	R	0xXX	

* The initial value of XSEL is determined by the settings of the XSEL1 and XSEL0 pins.

9.9 Synchronization Sequence

9.9.1 Sequence Control

Through sequence control, mode detection, FFT window detection, carrier recovery, clock recovery, and frame synchronization detection are automatically performed. The statuses in the synchronization sequence are as follows. The status can be monitored by the seqen register. (Refer to Section 9.17.)

seqen = 0: Transmission mode detection
seqen = 1: FFT window position initial pull-in
seqen = 2: Carrier AFC coarse synchronization
seqen = 3: Carrier AFC fine synchronization, clock AFC (first gain)
seqen = 4: Carrier AFC fine synchronization, clock AFC (second gain)
seqen = 5: Clock PLL (first gain)
seqen = 6: Clock PPL (second gain) (in 3/1-segment mode)
seqen = 7: Clock PPL (third gain) (in 3/1-segment mode)
seqen = 8: Waiting for FFT window search completion
seqen = 9: Synchronization sequence completion

【[Important] **The period before TS error free at the time of channel switching is so shortened that it may sometimes be shorter than the frame synchronized FLOCK or seqen=8 or 9. The decision of reception completion should be made based on RLOCK (decision that no TS packet continuous error is found) rather than FLOCK and seqen.**

9.9.2 Initial Wait Time Setting

The wait time until the synchronization pull-in sequence starts is set with register syini_tim. The time to be set is expressed by the following equations:

Wait time = syini_tim x 2.016 [ms] (Equation 9-9-1)

By the start of the sequence process, the input signal level and frequency must be stabilized to normal states. Set the value taking into consideration the tuner local oscillator PLL synthesizer synchronization time and AGC convergence time, etc.

9.9.3 Automatic Detection of Transmission Mode

TC90512 automatically detects the effective symbol length (FFT size) and guard ratio of received signals. If any unused transmission mode is known in advance, the specified mode detection process can be skipped by setting the symds_off register as shown below. Note, however, the register cannot be set to skip all processes.

symds_off[11] =1: Mode 3, guard 1/4 skipped
symds_off[10] =1: Mode 3, guard 1/8 skipped
symds_off[9] = 1: Mode 3, guard 1/16 skipped
symds_off[8] = 1: Mode 3, guard 1/32 skipped
symds_off[7] = 1: Mode 2, guard 1/4 skipped
symds_off[6] = 1: Mode 2, guard 1/8 skipped
symds_off[5] = 1: Mode 2, guard 1/16 skipped
symds_off[4] = 1: Mode 2, guard 1/32 skipped
symds_off[3] = 1: Mode 1, guard 1/4 skipped
symds_off[2] = 1: Mode 1, guard 1/8 skipped
symds_off[1] = 1: Mode 1, guard 1/16 skipped
symds_off[0] = 1: Mode 1, guard 1/32 skipped

In addition, if the transmission mode is already known, the synchronization time can be shortened by setting "1" in the mdetsel register and the FFT size and guard length in the ffsize and gdleng registers. Even if the registers are set as described above in advance, the transmission mode is automatically searched if the set transmission mode does not match the transmitted signal.

9.9.4 FFT Window Position Setting

The FFT window is searched for automatically and placed at the position where the S/N ratio becomes largest after demodulation. This applies to the guard ratio 1/4 in Mode3 in which the guard period is longest. Even if multipath exists outside the guard, an optimum FFT window position is set automatically. Further, TC90512 can continuously perform FFT window control even after the initial search, so it is not necessary to search the FFT window position again even if input conditions change. Note, however, that **the FFT window continuous control is not performed when the intersymbol interference canceler ISIC is suppressing the multipath outside the guard.**

The schnum register is used to set the update cycle of the FFT window position continuous control. The initnum setting value is used instead of the schnum setting at pull-in immediately after demodulation reset.

FFT window automatic search one-step time interval (steady operation)
- Mode1: schnum x 4 x 48 [OFDM symbol]
- Mode2: schnum x 2 x 48 [OFDM symbol]]
- Mode3: schnum x 1 x 48 [OFDM symbol]]
- * When schnum = 0, 6 [OFDM symbol] is assumed regardless of what mode has been set.

FFT window automatic search one-step time interval (pull-in)
- Mode1: initnum x 4 x 12 [OFDM symbol]
- Mode2: initnum x 2 x 12 [OFDM symbol]
- Mode3: initnum x 1 x 12 [OFDM symbol]
- * When initnum = 0, 6 [OFDM symbol] is assumed regardless of what mode has been set.

* The unit [effective symbol] is the OFDM symbol period excluding the guard period.

9.9.5 Carrier Recovery/Clock Recovery Time Setting

Each sequence time of carrier AFC coarse/fine synchronization, clock AFC and PLL can be set.
The carrier AFC course synchronization time can be set by the md1_cpd, md2_cpd, and md3_cpd registers. For the carrier AFC fine synchronization and clock AFC, two-step gain switching is possible. The sequence time for each gain is set by the afctim_1 and afctim_2 registers. The time to be set is expressed by the following equations:

Mode1: Time = afctim_1 or afctim_2 x 16 [symbols]
Mode2: Time = afctim_1 or afctim_2 x 8 [symbols]
Mode3: Time = afctim_1 or afctim_2 x 4 [symbols]

For clock PLL in 3/1-segment mode, three-step (two steps at pull-in and one step at synchronization retention) gain switching is possible. The sequence time for each gain at pull-in is set by the plltim_1 and plltim_2 registers. The time to be set is expressed by the following equations:

Mode1: Time = plltim_1 or plltim_2 x 34 [symbols]
Mode2: Time = plltim_1 or plltim_2 x 18 [symbols]
Mode3: Time = plltim_1 or plltim_2 x 10 [symbols]

9.9.6 Setting Frame Synchronization Protection

Frame synchronization is detected with the synchronous word contained in TMCC. The synchronization protection period for frame synchronization is set with register fdtmax and the period to be set is expressed by the following formula. Note that a value any value from 0 to 3 cannot be set in fdtmax.

Mode 1: Synchronization protection period = fdtmax x 4 [frames]
Mode 2: Synchronization protection period = fdtmax x 2 [frames]

Mode 3: Synchronization protection period = fdtmax x 1 [frames]

When the synchronous word cannot be continually detected in the period of the set number of frames, non-synchronization is identified and pull-in is performed once again. The frame synchronization flag can be monitored by the FLOCK pin ("1" for synchronization state) the fulock register ("0" for synchronization state).

9.9.7 Sequence Retry Error Detection

TC90512 contains a built-in synchronization error detection function, allowing you to perform re-pull-in (retry) processing without waiting for frame synchronization assessment. When the number of retries for synchronization sequence re-pull-in increases to a value larger than the set value, "1" is output to the retryov register. Therefore, it is possible to detect quickly that unreceivable signals have been input by monitoring this flag.
Retries are decided when a C/N error, etc. is detected by monitoring the operation status of each sequence or when a particular sequence does not complete in a predetermined time, thus causing a timeout error. When the mdetsel register is set to "1" and the transmission mode is preset, the first retry is not counted to allow a mismatch of presets (caused by an error) to be excluded.

9.9.8 Reduction Pull-In Time by Presetting of Transmission Mode and TMCC

TC90512 is provided with functions to preset the mode/guard ratio and TMCC. The pull-in time at channel switching can be reduced by using these functions.

1) Mode/guard ratio

The search time for the mode/guard ratio can be saved by the preset function. With register mdetsel="1" set the mode and guard ratio to the ffsize and gdleng registers, respectively. When fulock="0," the values read from ffsize and gdleng can be used as values to be preset. (fulock can be used as not only the frame synchronization flag but also the SP detection flag. When SP detection is selected, the decision time decreases. If fulock="0" at SP detection, the mode and guard ratio are read correctly.) When register mdetsel ="1" is set, search is performed automatically even if wrong values are preset for the mode and guard ratio.

2) TMCC preset

TMCC data can be preset to each register at addresses B2h to B8h. The TMCC acquisition time that is two frame periods can be reduced. The values read from addresses B2h to B9h can be used as values to be preset. Be sure to use the TMCC non-detection flag tmunvld="0" in advance to confirm that the correct TMCC data is obtained. Even if incorrect TMCC data is preset, it is automatically corrected to the correct value. In this case, however, the pull-in time is not decreased. The following parameters, which are frequently used for usual broadcasting services, are set as the initial values at B2h to B8h.

Mode 3, guard ratio 1/8
Layer A: Partial reception 1-segment, QPSK, coding rate 2/3, time interleave length I=4
Layer B: 12-segment, 64QAM, coding rate 3/4, time interleave length I=2

In addition, the time to TS error free can be reduced by presetting the value monitored by eqqdt to eqqth. This function should be used together with TMCC preset. (Refer to Sections 9.15 and 9.17.)

Name	Address (HEX)	Data	R/W	Initial Value	Description
syini_tim [7:0]	3A	[7:0]	W	0x10	Initial wait time setting Sets the initial wait time until synchronization pull-in begins. Wait time = syini_tim x 2.016 [ms]
retrycnt [3:0]	3B	[7:4]	W	0x1	Retry count threshold value (retry over) setting Number of retries to decide retry over at synchronization pull-in If the number of retries is larger than the set value, retryov = "1" is output.
symds_off [11:8]	3B	[3:0]	W	0x0	Transmission mode search restriction setting symds_off[11] = 1: Mode 3, guard 1/4 skipped symds_off[10] = 1: Mode 3, guard 1/8 skipped symds_off[9] = 1: Mode 3, guard 1/16 skipped symds_off[8] = 1: Mode 3, guard 1/32 skipped symds_off[7] = 1: Mode 2, guard 1/4 skipped symds_off[6] = 1: Mode 2, guard 1/8 skipped symds_off[5] = 1: Mode 2, guard 1/16 skipped symds_off[4] = 1: Mode 2, guard 1/32 skipped symds_off[3] = 1: Mode 1, guard 1/4 skipped symds_off[2] = 1: Mode 1, guard 1/8 skipped symds_off[1] = 1: Mode 1, guard 1/16 skipped symds_off[0] = 1: Mode 1, guard 1/32 skipped
symds_off [7:0]	3C	[7:0]	W	0x00	
cdtref [7:0]	3D	[7:0]	W	0x10	Amplitude decision threshold setting of correlation detection 0: Minimum to 255: Maximum
ofsref [7:0]	3E	[7:0]	W	0x08	Decision threshold setting for correlated interference detection 0: Minimum to 255: Maximum
afctim_1 [7:0]	3F	[7:0]	W	0x0C	Carrier/Clock AFC first gain sequence length setting Mode 1: Time = afctim_1 x 16 [symbols] Mode 2: Time = afctim_1 x 8 [symbols] Mode 3: Time = afctim_1 x 4 [symbols]
afctim_2 [7:0]	40	[7:0]	W	0x0C	Carrier/Clock AFC second gain sequence length setting Mode 1: Time = afctim_2 x 16 [symbols] Mode 2: Time = afctim_2 x 8 [symbols] Mode 3: Time = afctim_2 x 4 [symbols]
plltim_1 [7:0]	41	[7:0]	W	0x00	Clock PLL first gain sequence length setting Enabled in 3/1-segment mode only. Mode 1: Time = plltim_1 x 34 [symbols] Mode 2: Time = plltim_1 x 18 [symbols] Mode 3: Time = plltim_1 x 10 [symbols]
plltim_2 [7:0]	42	[7:0]	W	0x00	Clock PLL second gain sequence length setting Enabled in 3/1-segment mode only. Mode 1: Time = plltim_2 x 34 [symbols] Mode 2: Time = plltim_2 x 18 [symbols] Mode 3: Time = plltim_2 x 10 [symbols]
fmax_ini [3:0]	43	[7:4]	W	0x4	Number of protected synchronizations for frame synchronization at pull-in The timer starts in sequence 3. Synchronization protection period = fmax_ini [frames]
fdtmax [3:0]	43	[3:0]	W	0xF	Number of synchronization protection frames for frame synchronization Mode 1: Synchronization protection period = fdtmax x 4 [frames] Mode 2: Synchronization protection period = fdtmax x 2 [frames] Mode 3: Synchronization protection period = fdtmax [frames] * 0 to 3 cannot be set.

ndtmax [3:0]	44	[3:0]	W	0xF	Synchronization protection period for C/N error decision 13-segment Mode 1: Synchronization protection period = ndtmax x 420 [symbols] Mode2: Synchronization protection period = ndtmax x 210 [symbols] Mode3: Synchronization protection period = ndtmax x 105 [symbols] 3/1-segment Mode 1: Synchronization protection period = ndtmax x 52 [symbols] Mode 2: Synchronization protection period = ndtmax x 26 [symbols] Mode3: Mode 3: Synchronization protection period = ndtmax x 13 [symbols]
tlimsel [1:0]	46	[7:6]	W	0x0	Allowable range for timing synchronization decision 0: ±1/8 of guard period 1: ±1/4 of guard period 2: ±1/2 of guard period 3: ±guard period
mgthsel [1:0]	46	[5:4]	W	0x2	Correlated peak width decision threshold setting 0: Minimum to 3: Maximum
mdetsel	47	[7]	W	0x0	Selects whether or not mode search is to be performed at initial pull-in. 0: Mode search ON at initial pull-in 1: Mode search OFF at initial pull-in Note that mode search is performed at re-pull-in (retry).
mlocksel	47	[6]	W	0x0	fulock flag output switching 0: Frame synchronization flag 1: SP detection flag *Enabled for fulock only. Not reflected in FLOCK.
cnth [7:0]	48	[7:0]	W	0x90	C/N error decision threshold value setting 0: Minimum to 255: Maximum
md1_cpd [1:0]	49	[7:6]	W	0x3	Time constant selection (Mode 1) at carrier AFC coarse synchronization Increasing the setting value by 1 changes the time constant by 2 times. 0: Minimum time constant to 3: Maximum time constant
md2_cpd [1:0]	49	[5:4]	W	0x2	Time constant selection (Mode 2) at carrier AFC coarse synchronization Increasing the setting value by 1 changes the time constant by 2 times. 0: Minimum time constant to 3: Maximum time constant
md3_cpd [1:0]	49	[3:2]	W	0x1	Time constant selection (Mode 3) at carrier AFC coarse synchronization Increasing the setting value by 1 changes the time constant by 2 times. 0: Minimum time constant to 3: Maximum time constant
syimp_off	4A	[7]	W	0x0	ON/OFF selection for FFT timing control based on impulse response detection 0: ON 1: OFF (controlled by guard correlation only)
wlimsel [1:0]	4A	[5:4]	W	0x0	Guard correlation based FFT timing control sensitivity setting 0: Minimum to 3: Maximum
wslim [2:0]	4A	[3:1]	W	0x1	FFT window search limit setting FFT window position minimum value: Mode 1: Minimum value= (wslim+1)×[samples] Mode 2: Minimum value= (wslim+1)×8 [samples] Mode 3: Minimum value= (wslim+1)×16 [samples] FFT window position maximum value: Mode 1: Maximum value = Guard period - (wslim+1)×4 [samples] Mode 2: Maximum value = Guard period - (wslim+1)×8 [samples] Mode 3: Maximum value = Guard period - (wslim+1)×16 [samples] * The unit [sample] refers to the number of FFT clocks. * With a guard ratio of 1/16 or 1/32, wslim>=4 cannot be set.
syld_off	4B	[0]	W	0x0	FFT timing control ON/OFF ON OFF (used only at SP monitoring)

tdtmax [1:0]	4C	[7:6]	W	0x0	Timeout period setting for sequence 1 0: Maximum to 3: Minimum 13-segment Mode 1: Time = (tdtmax+4) x 18 [symbols] Mode 2: Time = (tdtmax+4) x 10 [symbols] Mode 3: Time = (tdtmax+4) x 10 [symbols] 1/3-segment Mode 1: Time = (tdtmax+4) x 34 [symbols] Mode 2: Time = (tdtmax+4) x 18 [symbols] Mode 3: Time = (tdtmax+4) x 10 [symbols]
cpdmax [1:0]	4C	[5:4]	W	0x0	Timeout period setting for sequence 2 0: Maximum to 3: Minimum Timeout period (13-segment) Mode1: Time = (cpdmax + 3) x 38 [symbols] (for md1_cpd=3) Mode2: Time = (cpdmax + 3) x 22 [symbols] (for md2_cpd=2) Mode3: Time = (cpdmax + 3) x 14 [symbols] (for md3_cpd=1) Timeout period (1-segment/3-segment) Mode1: Time = (cpdmax + 3) x 70 [symbols] (for md1_cpd=3) Mode2: Time = (cpdmax + 3) x 38 [symbols] (for md2_cpd=2) Mode3: Time = (cpdmax + 3) x 22 [symbols] (for md3_cpd=1)
spdmax [1:0]	4C	[3:2]	W	0x0	Timeout setting for SP detection (The timer starts in sequence 4.) 0: Maximum to 3: Minimum 0: Time = 16 [symbols] 1: Time = 32 [symbols] 2: Time = 48 [symbols] 3: Time = 60 [symbols]
tmdmax [1:0]	4C	[1:0]	W	0x0	Timeout setting for sequence 8 (The timer starts in sequence 3.) 0: Maximum to 3: Minimum Mode 1: Time = (tmdmax+4) x 4 [frames] Mode 2: Time = (tmdmax+4) x 2 [frames] Mode 3: Time = (tmdmax+4) [frames]
retryov	80	[7]	R	0xX	Synchronization pull-in retry over flag Outputs an error flag if the number of retries exceeds the retrycnt value. 0: Normal, 1: Error
woffset [7:0]	B1	[7:0]	R/W	0x02	FFT demodulation window position setting With the start of the effective period as the center, it is possible to set a value within a range that is 1/4 effective period before (woffset = 127) to 1/4 effective period after (woffset = -128). Mode 1: Window position = woffset x 4 [samples] Mode 2: Window position = woffset x 8 [samples] Mode 3: Window position = woffset x 16 [samples] * The unit [sample] refers to the number of FFT clocks.
schnum [3:0]	E4	[7:4]	W	0x8	FFT window continuous search one-step time interval 0: Minimum to 15: Maximum Mode 1: schnum x 4 x 48 [OFDM symbols] Mode 2: schnum x 2 x 48 [OFDM symbols] Mode 3: schnum x 1 x 48 [OFDM symbols] * When schnum = 0, 6 [OFDM symbol] is assumed regardless of what mode has been set.
initnum [3:0]	E4	[3:0]	W	0x4	FFT window automatic search one-step time interval (pull-in) 0: Minimum to 15: Maximum Mode 1: initnum x 4 x 12 [OFDM symbols] Mode 2: initnum x 2 x 12 [OFDM symbols] Mode 3: initnum x 1 x 12 [OFDM symbols] * When initnum = 0, 6 [OFDM symbol] is assumed regardless of what mode has been set.

* For the TMCC-related registers, refer to Section 9.17.

9.10 ISIC

TC90512 has a built-in **Intersymbol Interference Canceler (ISIC)**.
Because the FFT window position control function covers only the time period up to the guard period, it cannot remove intersymbol interferences that occur in long-delayed multipath outside the guard. The ISIC of TC90512 suppress the intersymbol interferences that occur in long-delayed multipath beyond the guard period (out-of-guard multipath), thereby improving the reception performance in deteriorated SFN environment. The ISIC can provide a suppression effect against long-delayed multipath that will cause preecho and postecho, making it possible to cope with multiple multipath waves.

The ISIC is set OFF by default. It is set ON by setting the sydfmd register to "1." When set ON, the ISIC operates automatically in accordance with the input condition, it need not be controlled from the outside. The conditions for which the ISIC operates are shown in the table below. The ISIC ON setting is invalid for the conditions to which the table shows that the ISIC is not applicable.

Table 9.5 Conditions to which ISIC is Applicable

condition	GI=1/32	GI=1/16	GI=1/8	GI=1/4
13segment	○	○	○	×
12+1segment	○	○	○	×
3segment	×	×	×	×
1 segment	×	×	×	×

* Differential segments are excluded. (The ISIC cannot be applied.)
* The ISIC is independent of the mode, time interleave length, modulation system, and coding rate.

[Important] The ISIC is set OFF by default. It is set ON by setting the register sydfmd="1" to effect the demodulation reset "imsrst."
The ISIC multipath suppression function does not operate with the FFT window continuous control function. However, when out-of-guard multipath does not exist, the ISIC stops automatically and the FFT window continuous control function begins operating.

Name	Address (HEX)	Data	R/W	Initial Value	Description
grgain [2:0]	7C	[2:0]	W	0x0	Filter factor correction gain for ISIC 0: x1 1: x3/4 2: x1/2 3: x3/8 4: x1/4 5: x3/16 6: x1/8 7: x3/32
gripklv [2:0]	7D	[6:4]	W	0x5	Differential detection threshold value within the guard 0: Minimum to 7: Maximum
gropklv [2:0]	7D	[2:0]	W	0x2	Differential detection threshold value outside the guard 0: Minimum to 7: Maximum
gract	7F	[3]	R	0x0	ISIC operation status monitor 0: OFF 1: ON
grovnum [2:0]	7F	[2:0]	R	0x0	Number of detected out-of-guard multipath waves
groff	C7	[6]	W	0x0	ISIC forced through 0: ISIC through unavailable, 1: ISIC forced through (for test purposes)
gr1dly [12:8]	C8	[4:0]	R	0x00	Filter 1 delay time for ISIC [12]: Precedence wave flag 0: Remove delayed waves. 1: Remove precedence waves. [11:0]: Delayed amount 0: No multipath 10: Minimum delay to 2750: Maximum delay
gr1dly [7:0]	C9	[7:0]	R	0x00	

gr2dly [12:8]	CA	[4:0]	R	0x00	Filter 2 delay time for ISIC [12]: Precedence wave flag 0: Remove delayed waves. 1: Remove precedence waves. [11:0]: Delayed amount 0: No multipath 10: Minimum delay to 2750: Maximum delay
gr2dly [7:0]	CB	[7:0]	R	0x00	
gr3dly [12:8]	CC	[5:0]	R	0x00	Filter 3 delay time for ISIC [12]: Precedence wave flag 0: Remove delayed waves. 1: Remove precedence waves. [11:0]: Delayed amount 0: No multipath 10: Minimum delay to 2750: Maximum delay
gr3dly [7:0]	CD	[7:0]	R	0x00	
sydfmd [1:0]	EF	[1:0]	W	0x0	ISIC/continuous FFT window search switch setting 0: ISIC OFF (Only FFT window continuous control is performed.) 1: ISIC ON 2: For test 3: Disabled * To enable the setting, perform demodulation reset imsrst.

9.11 FFT

TC90512 is provided with built-in 2k-, 4k- and 8k-point compatible FFT circuits, and utilizes a block floating decimal point operation to ensure internal operation accuracy in FFT processing. TC90512 contains a high-precision operation circuit to improve the carrier-to-interference performance.

9.12 CPE Removal

TC90512 effectively removes phase variation of input signals (**CPE**: Common Phase Error) caused by tuner phase noise, etc., in the time domain and frequency domain. The former is referred to as the **time CPE** and the latter as the **frequency CPE**.
The time CPE corrects the phase variation within the symbol period at the time domain prior to FFT.
The frequency CPE uses the continuous pilot signals between symbols to detect phase variations common to all carriers in the frequency domain after FFT and correct detected variations.
The time CPE removal operation can be set ON and OFF using the cpet_off register. The frequency CPE removal operation can be set ON and OFF using the cpe_off register.

Name	Address (HEX)	Data	R/W	Initial Value	Description
cpet_off	50	[7]	W	0x0	Time CPE removal ON/OFF setting 0: ON 1: OFF
cpe_off	50	[6]	W	0x0	Frequency CPE removal ON/OFF setting 0: ON 1: OFF

9.13 CVI/CSI

If the transmission channel is affected by frequency selectivity interference such as multi-path or fading, the error correction performance is improved with **CSI** (Channel State Information) estimated from the pilots.
If an interference wave such as co-channel interference by analog TV or any other spurious interference exists in a particular frequency, the interference is detected with **CVI** (Carrier Variance Information) and erasure correction is performed to improve characteristics. With CVI, the interference peak value and its frequency position are determined for each symbol and CW interference can be detected for each carrier.
Setting the frequency position (carrier number) in the monadr register enables reading of the interference level of a specific carrier after one symbol by the cvim register. Besides, the carrier position of the largest interference is monitored by cviloc and the largest interference amounts are monitored cvimax.
Further, the degree of multi-path or fading interference can be estimated from the temporal variation status of the transmission channel and calculated as frequency variation rate fvar and time variation rate tvar. TC90512 automatically optimizes error correction control by using these detection results.
PLR (pilot interference reduction) repairs the SP pilot effected by carrier interference to ease its influences. PLR is set ON by default and it regards multipath as carrier interference in deteriorated environments including multiwave multipath. Therefore, it is recommended to set OFF for normal operation.

Name	Address (HEX)	Data	R/W	Initial Value	Description
cvcnth [7:0]	51	[7:0]	W	0x68	C/N threshold value for CVI processing Threshold value for error operation prevention under low C/N conditions
csioff	52	[7]	W	0x0	ON/OFF for CSI processing Weighting by CSI (channel state Information) 0: ON 1: OFF
cvioff	52	[6]	W	0x0	ON/OFF for CVI processing Erasure correction (CVI) setting 0: ON 1: OFF
fdoff	52	[1]	W	0x0	Fading detection ON/OFF 0: ON 1: OFF
fdfm	52	[0]	W	0x0	Fading mode forced ON setting 0: OFF 1: ON
ofsd [7:0]	54	[7:0]	W	0x57	Fading detection offset setting 0: Minimum to FF: Maximum
scld [7:0]	55	[7:0]	W	0xF1	Fading detection slope setting 0: Minimum to FF: Maximum
tvth [7:0]	56	[7:0]	W	0x20	Fading detection time threshold setting 0: Minimum to FF: Maximum
fvth [7:0]	57	[7:0]	W	0x70	Fading detection frequency threshold setting 0: Minimum to FF: Maximum
plroff	5F	[7]	W	0x0	PLR processing ON/OFF 0: ON, 1: OFF (OFF for normal use)

9.14 Equalization

The coherent modulation carrier uses the transmission channel response estimated from the SP pilot signal for equalization. For the differential modulation carrier and TMCC carrier, differential detection is performed. TC90502 uses adaptive interpolation processing in SP pilot time and frequency for transmission channel response estimation, thereby establishing both the required C/N and time responsiveness. This adaptive control is performed automatically, eliminating the need for external control. Furthermore, pilot signals are used to monitor the C/N of received signals (demodulation S/N). The number of integration times at the time of detection is set to the cngsel register according to the required accuracy, and then read from cndat. To obtain the C/N (in decibels), perform conversion using the following equation:

$$C/N[dB] = 0.000024 \times P^4 - 0.0016 \times P^3 + 0.0398 \times P^2 + 0.5491 \times P + 3.0965 \qquad \text{(Equation 9-14-1)}$$
$$P = 10 \log(5505024 / cndat)$$

Obtained values contain errors due to signal processing, so they should be used as a guide. Note that detection methods with less errors are used for spurious and multipath interferences.

Name	Address (HEX)	Data	R/W	Initial Value	Description
eqcngsel [2:0]	4F	[2:0]	W	0x5	Pilot interpolation filter switching time interval setting 0: Maximum to 7: Minimum
cngsel [2:0]	5C	[6:4]	W	0x5	Average number of times for the C/N monitor 0: 65536 times 1: 32768 times 2: 16384 times 3: 8192 times 4: 4096 times 5: 2048 times 6: 1024 times 7: 512 times * Time required for C/N detection Mode 1: Average number of times/39 [symbols] Mode 2: Average number of times/39/2 [symbols] Mode 3: Average number of times/39/4 [symbols] (The number of times is 13 in 1-segment reception mode and 13/3 in 3-segment reception mode.)

* For monitor register details, refer to Section 9.17.

9.15 TMCC Detection

For the TMCC carrier, the majority decision is applied after differential detection and then the differential set cyclic code is decoded. The TMCC decoded data is output to addresses B2h to B9h on the register map. The TMCC decoding error flag is output to the tmunvld register. Note that when tmunvld="1", the TMCC decoded data is invalid.
If the TMCC signal is in the count-down state, the tmcchg register="1" is output. If the emergency alarm broadcasting start flag is "1", the emeflg register="1" is output.
By setting the cntdmax and cntumax registers, the cdunvld status register="1" is output over the specified frame period before and after count-down changeover. This status signal can be used as the mask signal if data collapses before and after count-down changeover.
For monitoring of the TMCC information, refer to the Read Register List in Section 9.17 "Monitor Output". These registers are R/W registers and can be used for TMCC presetting as well. (If the preset value differs from TMCC detection result, the preset value is replaced with the detection result.)

Name	Address (HEX)	Data	R/W	Initial Value	Description
eqqth [2:0]	4F	[7:5]	W	0x0	TMCC reserved area decision threshold value 0: Bit 122 to 6: Bit 128it, 7: Reserved area detection OFF
cntdmax [3:0]	5C	[3:0]	W	0x0	Mask signal cdunvld period setting before count-down Period=cntdmax x frame period
cntumax [5:0]	5D	[5:0]	W	0x0	Mask signal cdunvld period setting after count-down Period=cntumax x frame period

* For monitor register details, refer to Section 9.17.

9.16 Error Correction

The error correction decoder consists of frequency and time de-interleave, de-mapping, bit de-interleave, de-puncture, Viterbi decoding, byte de-interleave, energy de-dispersal (descramble), RS decoding, and layer selection output. Byte de-interleave, energy de-dispersal and RS decoding can be turned ON/OFF through settings.

9.16.1 Various Settings for TS Output

With the following registers, the TS output format can be set:

1) TS output format

palonff:	Stops the TS parallel byte clock (RSCKO) of the parity period. (Clock only for 188-byte data is output.) However, the TS serial clock does not stop.
revck:	Inverts RSCKO.
chclkp:	Inverts the TS serial clock polarity.
laysel:	Replaces the specified layer with a null packet.
nuckz:	Stops the serial clock in the serial data output null packet period.

2) Valid flag related

nuval:	Turns the valid signal of the null packet OFF. (Excluding null packets actually transmitted)
anuval:	Does not set the valid signal of packets forcefully or automatically nullified when nuval = "1".
ipbval:	Inverts the polarity of the valid signal. ("1" in normal data period)

3) Error flag related

auto_nul:	Replaces all layers with null packets at threshold value or higher error occurrence.
msoff:	Does not change the second byte MSB error indicator in the TS packet.
asyncng:	Turns OFF the function that forcibly sets a TS packet (including null packet) error during the asynchronous period until demodulation pull-in completion.
rlocksw:	Selects RLOCK decision criteria. Either sets RLOCK with the TS packet continuously error free, or sets RLOCK with no errors during the period of one frame.

9.16.2 Layer Selection

When layers are multiplexed, the output at each layer can be changed to null packets by setting the established bit of the laysel[2:0] register to "1". In addition, with this setting it is possible to select and measure only a specific layer at the time of BER measurement at serial output. laysel[2], laysel[1] and laysel[0] correspond to layers A, B and C, respectively.
In the event error packets frequently occur due to reception status deterioration, packets of a specific layer can be made into null packets as well.

9.16.3 Serial Output for BER Measurement

Setting the beron register to "1" outputs the serial data and the serial clock for BER measurement instead of TS serial output. The data to be output is 187 bytes of data, excluding TS synchronization byte 47 and parity. (Excluding OFDM multiplexed null packets.)

9.16.4 RS Decoding ON/OFF

RS decoding can be turned ON and OFF with the rsoff register setting.

9.16.5 BER Monitor after Viterbi Decoding

With the cor register set to "1", the number of error bits corrected in RS decoding can be counted for each predetermined cycle. When the number of RS decoded bits can be approximated as equal to the number of error bits that remain after Viterbi correction, the number of error bits divided by the total number of bits in the measurement cycle is the BER value after Viterbi correction.

1) Selecting the measurement cycle mode

In ISDB-T, the number of TS packets per frame differs according to modulation parameters. Two measurement cycle modes are therefore provided: packet mode which specifies the total number of packets, and time mode which specifies the number of frames.

Packet mode: tsch="0"
Counts the number of errors (number of error bits when cor = "1") for each specified number of packets.

Time mode: tsch="1"
Counts the number of errors (number of error bits when cor = "1") for each specified number of frames.

2) Selecting the BER measurement layer

When measurement is conducted using an external BER measurement counter, the layer to be measured is set with the laysel register. When BER measurement is conducted using the TC90512 internal error counter, three layers can be measured simultaneously, thereby rendering layer selection unnecessary.

3) Setting the measurement cycle

The measurement cycle for both packet mode and time mode is set in the cyc[2:0] register.

Measurement Cycle Setting

Value	Packet mode	Time Mode (Mode1, Mode2)	Time Mode (Mode3)
0	512 packets	2 frames	0.5 frames
1	1024 packets	4 frames	1 frame
2	2048 packets	8 frames	2 frames
3	4096 packets	16 frames	4 frames
4	8192 packets	32 frames	8 frames
5	16384 packets	Cannot be set	16 frames
6	32768 packets	Cannot be set	Cannot be set

4) Reading the error count (number of bits)

Count value for layer A: Output to perra[23:0]
Count value for layer B: Output to perrb[23:0]
Count value for layer C: Output to perrc[23:0]

5) Reading the total number of packets of the measurement cycle

The number of packets specified in packet mode is the same as the setting value and therefore does not need to be read. In time mode, however, the number of packets in one frame differs according to transmission parameters. The total number of packets of the period of the number of frames specified with cyc can be read using the following register:

Total number of packets of layer A: Output to pecya[15:0]
Total number of packets of layer B: Output to pecyb[15:0]
Total number of packets of layer C: Output to pecyc[15:0]

6) Calculating BER after Viterbi decoding

The following formula can be used to approximately calculate BER after Viterbi decoding:

$$BER \approx perra / (pecya \times 204 \times 8) \quad \text{(Equation 9-15-1)}$$

For layer B or layer C, use perrb, perrc and pecyb, pecyc.

* The number of error bits cannot be identified when errors of 9 bytes or more exist but correction by RS decoding is not possible. For this reason, the approximate calculation result of the equation shown above is saturated at about 7.8×10^{-2}.

9.16.6 BER Monitor after RS Decoding

With the cor register set to "0" (default), the number of error packets (the number of packets with errors of 9 bytes or more that cannot be corrected by RS) after RS decoding can be counted for each setting period.
The packet error rate PER is calculated based on the ratio of the number of packets that cannot be corrected by RS to the total number of packets of the measurement cycle. BER is calculated on the supposition that the number of error bytes in a packet that cannot be corrected by RS is nine. (The probability of occurrence of an error of 10 bytes or more is presumed to be low.)

1) Selecting the measurement cycle mode

In ISDB-T, the number of packets per frame differs according to modulation parameters. Two measurement cycle modes are therefore provided: packet mode which specifies the total number of packets, and time mode which specifies the number of frames.

Packet mode: tsch="0"
Counts the number of errors (number of error packets when cor = “0”) for each specified number of packets.

Time mode: tsch="1"
Counts the number of errors (number of error packets when cor = “0”) for each specified number of frames.

2) Selecting the BER measurement layer

When measurement is conducted using an external BER measurement counter, the layer to be measured is set with the laysel register.
When BER measurement is conducted using the TC90512 internal error counter, three layers can be measured simultaneously, thereby rendering layer selection unnecessary.

3) Setting the measurement cycle

The measurement cycle for both packet mode and time mode is set in the cyc[2:0] register.

Measurement Cycle Setting

Value	Packet mode	Time Mode (Mode 1, Mode 2)	Time Mode (Mode 3)
0	512 packets	2 frames	0.5 frames
1	1024 packets	4 frames	1 frames
2	2048 packets	8 frames	2 frames
3	4096 packets	16 frames	4 frames
4	8192 packets	32 frames	8 frames
5	16384 packets	Cannot be set	16 frames
6	32768 packets	Cannot be set	Cannot be set

4) Reading the error count (number of packets)

Count value for layer A:	Output to perra[23:0]
Count value for layer B:	Output to perrb[23:0]
Count value for layer C:	Output to perrc[23:0]

5) Reading the total number of packets of the measurement cycle

The number of packets specified in packet mode is the same as the setting value and therefore does not need to be read. In time mode, however, the number of packets in one frame differs according to transmission parameters. The total number of packets of the period of the number of frames specified with cyc can be read using the following register:

Total number of packets of layer A:	Output to pecya[15:0]
Total number of packets of layer B:	Output to pecyb[15:0]
Total number of packets of layer C:	Output to pecyc[15:0]

6) Calculating BER after RS decoding

The following formula can be used to approximately calculate BER after RS decoding. For layers B and C, perrb, perrc and pecyb, pecyc are used.

PER ≈ perra / pecya (Equation 9-15-2)
BER ≈ (perra x 8 x 0.5 x 9) / (pecya x 204 x 8) (Equation 9-15-3)

* When RS correction is not possible, the number of error packets cannot be specified. A margin of error is therefore included.

9.16.7 Setting for Changing TS Output Packets to Null Packets at Hierarchical Modulation

(1) Layer forced null packet setting

A specific layer packet can be forcibly changed into a null packet with the laysel register. (Refer to Section 9.16.2.)

(2) Automatic null packet replacement at frequent error occurrence

When error packets frequently occur, malfunction due to PID misidentification, etc., may occur in the MPEG decoder. TC90512 prevents such malfunctions by automatically changing TS packets into null packets in accordance with the error occurrence frequency.

1) Setting the error count mode

When automatic null packet creation is to be used, set cor to "0" (counts errors based on the number of packets).

2) Setting the measurement cycle mode

Similar to the operation performed for BER measurement, select packet mode (packet unit) or time mode (frame unit). Note that the counter used for error measurement can be reset by jperst.

3) Setting the measurement cycle

Similar to the operation performed for BER measurement, set the cycle for error counting in the cyc register.

4) Specifying the layer for automatic null packet replacement

Automatic null packet creation is common to all layers, and is set by setting the auto_nul register to "1".

5) Setting the automatic null packet replacement ON/OFF threshold value

Set the threshold value for the error count. When this threshold value is exceeded, the TS output packet is replaced with a null packet. Hysteresis characteristics can be applied to the threshold value.
The threshold value for deciding “null packet replacement ON” is set in shsl[2:0] when the error count value increases, and the threshold value for deciding “null packet replacement OFF” is set in shsc[2:0] when the error count value decreases. To ensure that the hysteresis operation is properly performed, set the values so that shsl ≤ shsc. These threshold values are common to each layer.

* The threshold values shsc and shsl are set based on the ratio to the number of packets of the observation packet cycle pecya (a, b, c). Set the values so that the product of the two is 1 or greater. For instance, when the observation packet cycle is “384 packets” in packet mode and the settings are set so that shsc and shsl are “1/512 of the cycle,” the products shsc pecya (a, b, c) and shsl pecya (a, b, c) are less than 1 packet even if an error occurs in all packets, causing improper operation.

9.16.8 Error Flag

Error flag-related information is summarized below:

rulock: "1" if any one of the layers contains an error ("0" if no layers contain errors)
RLOCK: "1" if any one of the layers contain no error)
RERR: "1" if any one of the layers contains an error

That is, rulock and RERR are the same signals. Error flag-related information for each layer is summarized below:

rlocka, rlockb, rlockc: "1" if a layer pertinent to each of these signals exists and no error exists
rerra, rerrb, rerrc: "1" if a layer pertinent to each of these signals exists and errors also exist

rlocka, rlockb, and rlockc are the same as RLOCKA, RLOCKB, and RLOCKC, respectively. Similarly, rerra, rerrb, and rerrc are the same as RERRA, RERRB, and RERRC, respectively.

9.16.9 Setting RS Decoding Error Decision Flags

Either of the following two methods to check for errors can be selected by the rlocksw register. In addition, error assessment can also be performed for each layer by masking the errors of specific layers.

rlocksw="1": Assesses that an error is present when an RS decoding error occurs one or more times in the OFDM frame period.

rlocksw="0": Assesses that no error is present when RS decoding is continuously error free for at least the number of packets set in the okval[2:0] register. Also conversely assesses that an error occurred in TS output when RS decoding errors continuously occur for at least the number of packets set in the erval[2:0] register. (This assessment method is selected by default.)

RLOCK/RERR Assessment: No. of Continuous Faulty TS Packets

okval/erval	No. of Assessed Packets
0	1 (erval default value)
1	2
2	4
3	8 (okval default value)
4	16
5	32
6	64
7	128

9.16.10 Layer Identification Signal Output

The layer identification signal HSEL[1:0] can be synchronized with the TS packet and output to an output pin.

HSEL="0": Layer A packet
HSEL="1": Layer B packet
HSEL="2": Layer C packet
HSEL="3": Null packet

9.16.11 Error Identification, BER Measurement and Null Packet Replacement Relationship

Figure 9.8 shows the correlation between the error flags, BER measurement and null packet replacement settings.
RSEORF is generated by using an error on a packet-by-packet basis. The result of RLOCK can be reflected on RSEORF, or the final TS packet error flag. This is intend for suppressing the unstable state (or alternate occurrence of 1 and 0 during the course of synchronization pull-in) of the TS error flag.
On the other hand, BER measurement and the null packet replacement process use the error counter result. In conjunction with null packet replacement, the valid signal can also be linked using nuval and anuval.

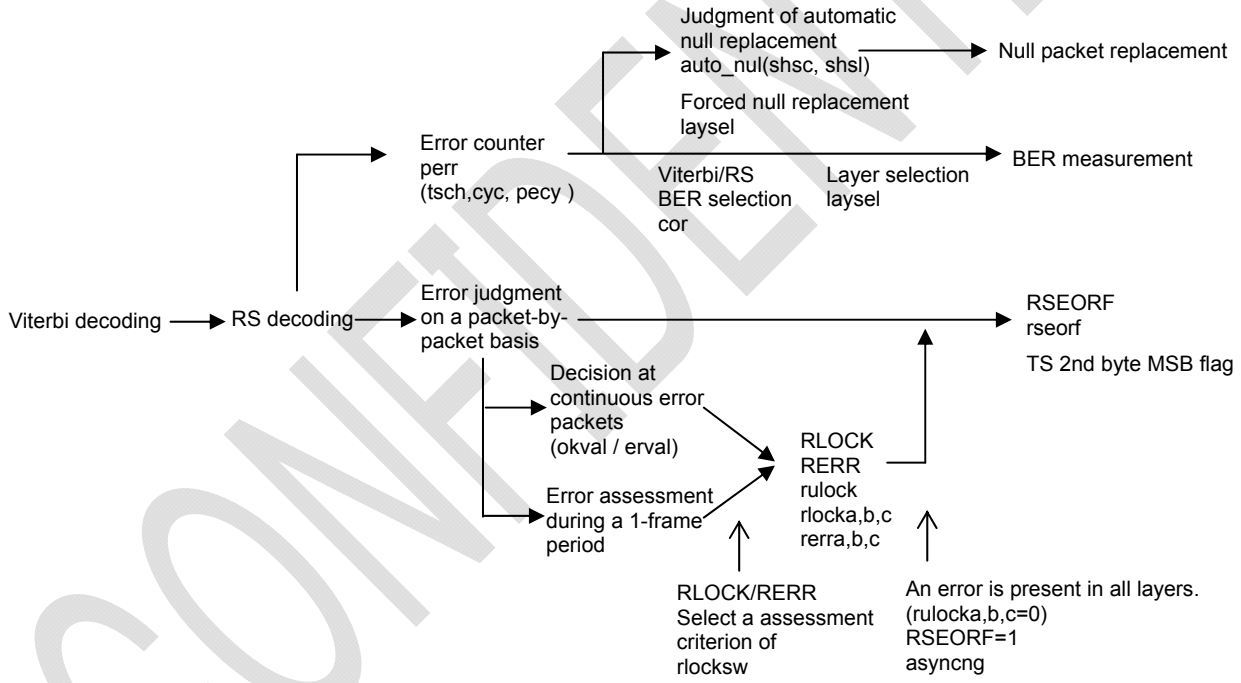


Fig. 9.8 Setting the Error Flag

Name	Address (HEX)	Data	R/W	Initial Value	Description
dintoff	70	[7]	W	0x0	Byte de-interleave OFF setting 0: ON 1: OFF
dscroff	70	[6]	W	0x0	Energy dispersal descramble OFF setting 0: ON 1: OFF
okval [2:0]	70	[5:3]	W	0x3	RLOCK/RERR number of continuous error free TS packets okrval: No. of Assessed Packets 0: 1 1: 2 2: 4 3: 8 (okval default value) 4: 16 5: 32 6: 64 7: 128
erval [2:0]	70	[2:0]	W	0x0	RLOCK/RERR number of continuous TS packets with errors erval: No. of Assessed Packets 0: 1 (erval default value) 1: 2 2: 4 3: 8 4: 16 5: 32 6: 64 7: 128
rsoff	71	[7]	W	0x0	RS decoding OFF setting 0: 0: ON, 1: OFF (for test)
revck	71	[6]	W	0x0	RSCKO clock inversion Inverts the TS parallel output byte clock (RSCKO). 0: Normal, 1: Inversion
palonff	71	[5]	W	0x0	RSCKO setting 0: Issue clock during the parity period as well (204 bytes) 1: Stop clock during the parity period (188 bytes)
ipbval	71	[4]	W	0x0	Valid polarity inversion 0: Data period "1", parity period "0" 1: Parity period "1", data period "1"
msoff	71	[3]	W	0x0	TS packet 2nd MSB error flag setting 0: Set to 1 with error (normal) 1: Through (no flag change)
laysel [2:0]	71	[2:0]	W	0x0	Replacement of specified layer with null packet [2]: Layer A, [1]: Layer B, [0]: Layer C 0: Do not replace with a null packet 1: Replace with a null packet.
rmsk [2:0]	72	[4:2]	W	0x0	RLOCK/RERR flag mask setting [2]: Layer A, [1]: Layer B, [0]: Layer C 0: Do not mask, 1: Mask * rmsk is used to forcibly set rlocka, rlockb, and rlockc (RLOCKA, RLOCKB, and RLOCKC) to 1, and rerra, rerrb, and rerrc (RERRA, RERRB, and RERRC) to 0 when a layer exists.
beron	75	[6]	W	0x0	Serial output switching 0: TS serial data/clock 1: BER measurement serial data/clock
rlocksw	75	[5]	W	0x0	RLOCK/RERR assessment criteria selection 0: Assessment at continuous packet error (threshold values okval, erval) 1: Assessment during one frame period (TC90A87 compatible)
nuckz	75	[3]	W	0x0	Clock stoppage at serial TS output null packet 0: OFF, 1: ON (Clock is stopped.)
chclkp	75	[1]	W	0x0	Inverts the serial TS output clock polarity. 0: Data (SRDT) and clock (SRCK) rising edge match 1:Inversion

auto_nul	76	[7]	W	0x0	Automatic creation of null packet setting Changes the layer to a null packet when the error counter value equals the threshold value shsc/shsl and the errors have been assessed as major. 0: OFF 1: ON
cyc [2:0]	76	[6:4]	W	0x0	Measurement cycle setting Value: Packet mode / Time mode (Modes 1 and 2) / Time mode (mode 3) 0: 512 packets / 2 frames / 0.5 frames 1: 1024 packets / 4 frames / 1 frames 2: 2048 packets / 8 frames / 2 frames 3: 4096 frames / 16 frames / 4 frames 4: 8192 packets / 32 frames / 8 frames 5: 16384 packets / Cannot be set / 16 frames 6: 32768 packets / Cannot be set / Cannot be set 7: Cannot be set / Cannot be set / Cannot be set
nuval	76	[3]	W	0x0	Null packet period valid flag setting Sets the valid flag of OFDM multiplexed null packets, including null packet creation based on layer selection, to OFF. (Null packets contained in data are excluded) 0: Valid flag on 1: Valid flag off
anuval	76	[2]	W	0x0	Valid flag setting for automatic/forced null packet replacement When nuval = "1," the valid flag for automatic and forced null packet replacement does not turn on. 0: Valid flag on 1: Valid flag off
asyncng	76	[1]	W	0x1	TS packet error setting at demodulation pull-in setting Turns ON the function that forcibly sets a TS packet (including null packet) error when rulock=1 in all layers. 0: Forcibly set error during asynchronous period 1: Do not forcibly set error during asynchronous period
perst	76	[0]	W	0x0	Forced resetting of the RS decoding error count "perra/b/c" in all layers 0: Do not reset. 1: Reset.
shsc [2:0]	77	[7:5]	W	0x0	Threshold value setting of automatic null packet replacement (null packet replacement stop) Threshold value for assessing "null packet replacement OFF" when error count increases Value: Threshold value 0: 1/8 of the cycle 1: 1/16 of the cycle 2: 1/32 of the cycle 3: 1/64 of the cycle 4: 1/128 of the cycle 5: 1/256 of the cycle 6: 1/512 of the cycle 7: Error counter value=1
shsl [2:0]	77	[4:2]	W	0x0	Threshold value setting of automatic null packet replacement (null packet replacement start) Threshold value for assessing "null packet replacement ON" when error count increases Value: Threshold value 0: 1/8 of the cycle 1: 1/16 of the cycle 2: 1/32 of the cycle 3: 1/64 of the cycle 4: 1/128 of the cycle 5: 1/256 of the cycle 6: 1/512 of the cycle 7: Error counter value=1

tsch	77	[1]	W	0x0	Measurement cycle setting of number of error packets 0: Packet mode 1: Time mode:
cor	77	[0]	W	0x0	Error measurement mode setting 0: No. of error packets after RS decoding count mode 1: No. of error packets after Viterbi decoding count mode

9.17 Monitor Output

The reception mode (FFT size, guard length), FFT window position, TMCC information and various reception states can be monitored. In addition, constellation and spectrum can be observed.

9.17.1 Reception Mode

Reception mode (FFT size, guard ratio) is automatically set by default and output to the ffsize and gdleng registers.

9.17.2 Constellation/SP (Spreading Pilot) Signal Monitor

The I-axis data and Q-axis data of the constellation and SP signals are output to the mondati and mondatq registers, respectively. Constellation/SP signal changeover is performed with the monsel register.

(1) Constellation monitor

When monsel = “0”, constellation output (equalization output) is set.
The carrier number to be monitored is set with the monadr register. The following indicates the range of valid carrier numbers for constellation monitoring. After the carrier number is set in monadr and data is updated after a waiting period of one symbol or longer, the I-axis and Q-axis data are read from mondati and mondatq.

[13-segment]
Mode1: 322 - 1726
Mode2: 644 - 3452
Mode3:1288 - 6904

[1-segment]
Mode1: 970 - 1078
Mode2: 1940 - 2156
Mode3: 3880 - 4312

[3-segment]
Mode1: 862 - 1186
Mode2: 1724 - 2372
Mode3: 3448 - 4744

(2) SP monitor

When SP (spreading pilot) signals are arranged and observed in the direction of frequency, the frequency characteristics of the transmission channel can be observed in an approximate manner. In addition, when the SP signal is converted with Inversed DFT, a delay profile can be obtained.
With monsel=”1”, SP output (FFT output) is set. For the carrier number of the SP signal to be output, set the value calculated using the formula below in the monadr register. (Other monadr values result in invalid data output.)
Since the SP signal continually changes, set the sp_hold register to "1" (the SP signal is updated) at least 100ms after stopping FFT timing control by setting the syld_off register to "1", and then read the SP signal.

* When the sp_hold register is set to "1", writing to IC internal SP memory is stopped and normal TS output cannot be obtained.

[13-segment]

monadr = 322 + 3 x n_sp (Mode1)
= 644 + 3 x n_sp (Mode2)
= 1288 + 3 x n_sp (Mode3) (Equation 9-17-1)

n_sp: SP number
n_sp=0, 1, 2,…, 467 (Mode 1) in the order of low frequency to high frequency
n_sp = 0,1,2,…,935 (Mode2)
n_sp = 0,1,2,…,1871 (Mode3)

[1-segment]

monadr = 970 + 3 x n_sp (Mode1)
= 1940 + 3 x n_sp (Mode2)
= 3880 + 3 x n_sp (Mode3) (Equation 9-17-2)

n_sp: SP number
n_sp=0, 1, 2,…, 36 (Mode 1) in the order of low frequency to high frequency
n_sp = 0,1,2,…,72 (Mode2)
n_sp = 0,1,2,…,144 (Mode3)

[3-segment]

monadr = 862 + 3 x n_sp (Mode1)
= 1724 + 3 x n_sp (Mode2)
= 3448 + 3 x n_sp (Mode3) (Equation 9-17-3)

n_sp: SP number
n_sp=0, 1, 2,…, 108 (Mode 1) in the order of low frequency to high frequency
n_sp = 0,1,2,…,216 (Mode2)
n_sp = 0,1,2,…,432 (Mode3)

9.17.3 TMCC Decoded Data

OFDM demodulation TMCC decoded data is output to the registers of addresses b2h to b9h. This data is only valid if the tmuvld register (address 80h) is "0".

Name	Address (HEX)	Data	R/W	Initial Value	Description
retryov	80	[7]	R	0xX	Synchronization pull-in retry over flag Outputs an error flag if the number of retries exceeds the retrycnt value. 0: Normal, 1: Error
alarm	80	[6]	R	0xX	Reception level error flag 0: Normal, 1: Error
tmunvld	80	[5]	R	0xX	TMCC non-detection flag 0: Detected, 1: Not detected
mdunvld	80	[4]	R	0xX	recvmd setting error flag 0: Normal, 1: Error
fulock	80	[3]	R	0xX	Frame non-synchronization flag 0: Synchronized, 1: Not synchronized * SP detection flag (0: Normal, 1: Error) set with mlocksel="1".
vulock	80	[2]	R	0xX	Viterbi synchronization error flag 0: Normal, 1: Error
rulock	80	[1]	R	0xX	RS decoding error flag 0: Normal, 1: Error * The error presence assessment method can be selected with rlocksw. rlocksw ="0": Frame unit rlocksw ="1": TS packet unit * When rmsk is used, only the result of a specific layer can be reflected.
rseorf	80	[0]	R	0xX	TS packet error flag Flag indicating the presence/absence of an RS uncorrectable error of 9 bytes or more 0: Normal, 1: Error

emerg	81	[7]	R	0xX	TMCC emergency alarm broadcasting start flag 0: Start not controlled, 1: Start controlled
tmcchg	81	[6]	R	0xX	TMCC count-down flag 0: Count-down not provided, 1: Count-down provided
cdunvld	81	[5]	R	0xX	Flag indicating mask period before and after TMCC count-down 0: No mask period, 1: Mask period
slpen	81	[4]	R	0xX	Flag indicating sleep/wakeup mode 0: Sleep mode, 1: Wakeup mode
ifagc_dt [7:0]	82	[7:0]	R	0xXX	IF_AGC control level monitor output Indicates the IF_AGC control volume. (SB format)
rfagc_dt [7:0]	83	[7:0]	R	0xXX	RF_AGC control level monitor output Indicates the RF_AGC control volume. (SB format)
carafc_dt [15:8]	84	[7:0]	R	0xXX	Carrier frequency error monitor output Indicates the carrier frequency error. (2's complement format) When the receiver frequency is high, a negative (-) frequency error is output. When the receiver frequency is low, a positive (+) frequency error is output.
carafc_dt [7:0]	85	[7:0]	R	0xXX	
clk_afc [15:8]	86	[7:0]	R	0xXX	Carrier frequency error monitor output Indicates the clock frequency error. (2's complement format)
clk_afc [7:0]	87	[7:0]	R	0xXX	
mondati [7:0]	89	[7:0]	R	0xXX	Carrier I data output monsel = 0: Constellation output I data (I data equalization output set with monadr[12:0]) monsel=1: SP signal I data (I data FFT output set with monadr[12:0])
mondatq [7:0]	8A	[7:0]	R	0xXX	Carrier Q data output monsel = 0: Constellation output Q data (I data equalization output set with monadr[12:0]) monsel=1: SP signal Q data (Q data FFT output set with monadr[12:0])
cndat [23:16]	8B	[7:0]	R	0xXX	Constellation distributed data output Outputs the differential average value from the constellation reference point after equalization.
cndat [15:8]	8C	[7:0]	R	0xXX	
cndat [7:0]	8D	[7:0]	R	0xXX	
fvar [7:0]	8E	[7:0]	R	0xXX	Frequency variation rate monitor
tvar [7:0]	8F	[7:0]	R	0xXX	Time variation rate monitor
eqqdt [2:0]	90	[7:5]	R	0xXX	TMCC reserved area detection result 0: Bit 122 to 6: Bit 128it, 7: Reserved area not detected
cvimax [11:8]	90	[3:0]	R	0xXX	CVI interference volume monitor Outputs the maximum value of each symbol.
cvimax [7:0]	91	[7:0]	R	0xXX	
cviloc [12:8]	92	[4:0]	R	0xXX	CVI interference position monitor Outputs the cvimax carrier position.
cviloc [7:0]	93	[7:0]	R	0xXX	
fddet	94	[7]	R	0xX	Fading volume monitor Outputs the degree of fading from the time variation of FFT demodulation output.
cvim [11:8]	94	[3:0]	R	0xXX	CVI monitor of each carrier Outputs the CVI signal of the carrier number specified by monadr.
cvim [7:0]	95	[7:0]	R	0xXX	
rlocka	96	[7]	R	0xX	Layer A RS decoding error assessment 0: Error, 1: No error

rlockb	96	[6]	R	0xX	Layer B RS decoding error assessment 0: Error, 1: No error
rlockc	96	[5]	R	0xX	Layer C RS decoding error assessment 0: Error, 1: No error
verra [15:8]	97	[7:0]	R	0xXX	Viterbi decoding error count value of layer A
verra [7:0]	98	[7:0]	R	0xXX	
verrb [15:8]	99	[7:0]	R	0xXX	Viterbi decoding error count value of layer B
verrb [7:0]	9A	[7:0]	R	0xXX	
verrc [15:8]	9B	[7:0]	R	0xXX	Viterbi decoding error count value of layer C
verrc [7:0]	9C	[7:0]	R	0xXX	
perra [23:16]	9D	[7:0]	R	0xXX	Layer A RS decoding error count
perra [15:8]	9E	[7:0]	R	0xXX	
perra [7:0]	9F	[7:0]	R	0xXX	
perrb [23:16]	A0	[7:0]	R	0xXX	Layer B RS decoding error count
perrb [15:8]	A1	[7:0]	R	0xXX	
perrb [7:0]	A2	[7:0]	R	0xXX	
perrc [23:16]	A3	[7:0]	R	0xXX	Layer C RS decoding error count
perrc [15:8]	A4	[7:0]	R	0xXX	
perrc [7:0]	A5	[7:0]	R	0xXX	
pecya [15:8]	A6	[7:0]	R	0xXX	Layer A error count cycle (number of packets)
pecya [7:0]	A7	[7:0]	R	0xXX	
pecyb [15:8]	A8	[7:0]	R	0xXX	Layer B error count cycle (number of packets)
pecyb [7:0]	A9	[7:0]	R	0xXX	
pecyc [15:8]	AA	[7:0]	R	0xXX	Layer C error count cycle (number of packets)
pecyc [7:0]	AB	[7:0]	R	0xXX	
s_infom	AC	[4]	R	0xX	S_INFO signal monitor output
agcim	AC	[1]	R	0xX	AGCI signal monitor output
wunvld	AD	[7]	R	0x0	FFT window search completion 0: Search completed 1: Search not completed
ffsize [1:0]	B0	[7:6]	R/W	0x2	FFT size monitor output 0: 2048 1: 4096 2: 8192
gdleng [1:0]	B0	[5:4]	R/W	0x2	Guard ratio monitor output 0: 1/32 1: 1/16 2: 1/8 3: 1/4

seqen [3:0]	B0	[3:0]	R/W	0x0	Synchronization sequence status information 0: Transmission mode detection 1: FFT window initial pull-in 2: Carrier AFC coarse synchronization 3: Carrier AFC fine synchronization, clock AFC (first gain) 4: Carrier AFC fine synchronization, clock AFC (second gain) 5: Clock PLL (first gain) 6: Clock PPL (second gain) (in 3/1-segment reception mode only) 7: Clock PPL (third gain) (in 3/1-segment reception mode only) 8: Waiting for FFT window search completion 9: Synchronization sequence completion
sysid [1:0]	B2	[7:6]	R/W	0x0	TMCC system identification 0: TV, 1: Sound, Others: Reserved
pachg [3:0]	B2	[5:2]	R/W	0xF	TMCC parameter changeover indicator 0xF: No switching, Others: Number of frames until switching * TMCC parameters are updated at the frame following pachg=0.
emeflg	B2	[1]	R/W	0x0	TMCC emergency alarm broadcasting start flag 0: Start not controlled, 1: Start controlled
part	B2	[0]	R/W	0x1	TMCC partial reception flag TV mode: 0: No partial reception, 1: Partial reception Sound mode: 0: 1-segment, 1: 3-segment
a_cnst [2:0]	B3	[7:5]	R/W	0x1	TMCC layer A carrier modulation scheme 0: DQPSK 1: QPSK 2: 16QAM 3: 64QAM 7: No layer, Other: Reserved
a_rate [2:0]	B3	[4:2]	R/W	0x1	TMCC layer A convolution coding rate 0: 1/2 1: 2/3 2: 3/4 3: 5/6 4: 7/8 7: No layer, Other: Reserved
a_ileav [2:1]	B3	[1:0]	R/W	0x3	TMCC layer A time interleave scheme Mode 1: 0: I=0 1: I=4 2: I=8 3: I=16 7: No layer, Other: Reserved Mode 2: 0: I=0 1: I=2 2: I=4 3: I=8 7: No layer, Other: Reserved Mode 3: 0: I=0 1: I=1 2: I=2 3: I=4 7: No layer, Other: Reserved
a_ileav [0]	B4	[7]	R/W		
a_seg [3:0]	B4	[6:3]	R/W	0x1	Number of segments used by layer A 0xF: No layer
b_cnst [2:0]	B4	[2:0]	R/W	0x3	TMCC layer B carrier modulation scheme 0: DQPSK 1: QPSK 2: 16QAM 3: 64QAM 7: No layer, Other: Reserved
b_rate [2:0]	B5	[7:5]	R/W	0x2	TMCC layer B convolution coding rate 0: 1/2 1: 2/3 2: 3/4 3: 5/6 4: 7/8 7: No layer, Other: Reserved
b_ileav [2:0]	B5	[4:2]	R/W	0x2	TMCC layer B time interleave scheme Mode 1: 0: I=0 1: I=4 2: I=8 3: I=16 7: No layer, Other: Reserved Mode 2: 0: I=0 1: I=2 2: I=4 3: I=8 7: No layer, Other: Reserved Mode 3: 0: I=0 1: I=1 2: I=2 3: I=4 7: No layer, Other: Reserved

b_seg [3:2]	B5	[1:0]	R/W	0xC	Number of segments used by layer B 0xF: No layer
b_seg [1:0]	B6	[7:6]	R/W		
c_cnst [2:0]	B6	[5:3]	R/W	0x7	TMCC layer C carrier modulation scheme 0: DQPSK 1: QPSK 2: 16QAM 3: 64QAM 7: No layer, Other: Reserved
c_rate [2:0]	B6	[2:0]	R/W	0x7	TMCC layer C convolution coding rate 0: 1/2 1: 2/3 2: 3/4 3: 5/6 4: 7/8 7: No layer, Other: Reserved
c_ileav [2:0]	B7	[7:5]	R/W	0x7	TMCC layer C time interleave scheme Mode 1: 0: I=0 1: I=4 2: I=8 3: I=16 7: No layer, Other: Reserved Mode 2: 0: I=0 1: I=2 2: I=4 3:I=8 7: No layer, Other: Reserved Mode 3: 0: I=0 1: I=1 2: I=2 3: I=4 7: No layer, Other: Reserved
c_seg [3:0]	B7	[4:1]	R/W	0xF	Number of segments used by layer C 0xF: No layer
phcomp [2]	B7	[0]	R/W	0x1	Linked transmission phase correction volume 0: -π/8 1: -2π/8 2: -3π/8 3: -4π/8 4: -5π/8 5: -6π/8 6: -7π/8 7: No correction
phcomp [1:0]	B8	[7:6]	R/W	0x3	
resva [5:0]	B8	[5:0]	R/W	0x3F	TMCC reservation
resvb [5:0]	B9	[7:2]	R/W	0x3F	
monadr [12:8]	BA	[4:0]	W	0x00	Carrier number to be monitored Sets the carrier number to be monitored with the constellation output, CVI interference level or SP signal. The range of valid carrier numbers is as follows: Mode1: 322 - 1726 Mode2: 644 - 3452 Mode3: 1288 - 6904
monadr [7:0]	BB	[7:0]	W	0x00	
sp_hold	BC	[7]	W	0x0	SP signal hold changeover Disables writing SP signals to memory. 0: Normal operation, 1: Hold operation (used during SP monitoring)
monsel	BC	[6]	W	0x00	Monitor signal changeover Selects the signal to be output to mondati and mondatq. 0: Constellation output 1: SP signal
dagc_dt [7:0]	DA	[7:0]	R	0x0	Digital AGC gain monitor Outputs the digital AGC gain in 2's complement format. "0" indicates no gain (standard state). A positive value is a gain greater than 0 and a negative value is a gain smaller than 0.

9.18 I^2C Through Mode

TC90512 is provided with the I^2C through control pins TNSCL and TNSDA for setting the digital terrestrial tuner.
The I^2C through mode is enabled by accessing register address "FEh". The enabled state is cleared at the stop condition after a series of data transfers has ended. (Refer to Section 5.1.)

Name	Address (HEX)	Data	R/W	Initial Value	Description
tnflg [7:0]	FE	[7:0]	W	0x00	Sets the address and subsequently the I2C bus through mode. [7:1]: Tuner slave address [0]: Write to tuner at "0" Read from tuner at "1"

10. Basic Frequency Setting Example List

Boldface items are set automatically by XSEL1 and XSEL0 or by default.

10.1 57MHz IF Mode (XT=25MHz)

XSEL1=0, XSEL0=0				Standard Clock (Crystal) Frequency [MHz]		
Item		Symbol	Unit	**25.400**	25.667	26.000
Master clock frequency		MD	[MHz]	**76.200**	77.000	78.000
OFDM	IF frequency	IF	[MHz]	**57.000**		
	Data frequency	FS	[MHz]	**65.015873**		
	Serial TS clock	f_{OFDM}	[MHz]	**38.100**	38.500	39.000
	Clock frequency pull-in range	Δf/f	[ppm]	**±208**	±206	±203
	Carrier frequency pull-in range	f_{AFC}	[kHz]	**±250**		
	Standard clock division ratio	iexdiv	HEX(DEC)	**0Bh (11)**	0Bh (11)	0Bh (11)
	PLL division ratio	ilpdiv	HEX(DEC)	**21h (33)**	21h (33)	21h (33)
	Clock frequency Offset correction	hkfrq	HEX(DEC)	**2C0Ah (11,274)**	2F31h (12,081)	3320h (13,088)
	Carrier frequency Offset correction	cpld_dt	HEX(DEC)	**0FA0h (4,000)**	0E21h (3,617)	0C4Fh (3,151)
	Carrier AFC loop gain correction	affrq	HEX(DEC)	**170h (368)**	177h (375)	17Fh (383)
	Digital filter	lpfsl	HEX(DEC)	**3h(3)**		
	Frequency polarity	f_inv	BIN	**1**		
PSK	Symbol rate	JFS	[MHz]	**28.860**		
	Serial TS clock	f_{PSK}	[MHz]	**60.960**	61.600	62.400
	Clock frequency pull-in range	$\Delta f/f_{jCLK}$	[ppm]	**±200**		
	Carrier frequency pull-in range	f_{jAFC}	[MHz]	**±5**		
	Clock frequency Offset correction	jhkfrq	HEX(DEC)	**51F6h (20,982)**	5583h (21,891)	59F2h (23,026)
	Carrier AFC loop gain correction	afcg	HEX(DEC)	**52h (82)**	51h (81)	50h (80)

10.2 57MHz IF Mode (XT=20MHz)

XSEL1=0, XSEL0=1				Standard Clock (Crystal) Frequency [MHz]		
Item		Symbol	Unit	20.480	**20.500**	20.750
Master clock frequency		MD	[MHz]	81.920	**82.000**	83.000
OFDM	IF frequency	IF	[MHz]	**57.000**		
	Data frequency	FS	[MHz]	**65.015873**		
	Serial TS clock	f_{OFDM}	[MHz]	40.960	**41.000**	41.500
	Clock frequency pull-in range	Δf/f	[ppm]	±194	**±194**	±191
	Carrier frequency pull-in range	f_{AFC}	[kHz]	**±250**		
	Standard clock division ratio	iexdiv	HEX(DEC)	08h (8)	**08h (8)**	08h (8)
	PLL division ratio	ilpdiv	HEX(DEC)	20h (32)	**20h (32)**	20h (32)
	Clock frequency Offset correction	hkfrq	HEX(DEC)	428Fh (17,039)	**42E0h (17,120)**	46D0h (18,128)
	Carrier frequency Offset correction	cpld_dt	HEX(DEC)	0DE0h (3,552)	**0E0Dh (3,597)**	1032h (4,146)
	Carrier AFC loop gain correction	affrq	HEX(DEC)	0D3h (211)	**0D4h (212)**	0DDh (221)
	Digital filter	lpfsl	HEX(DEC)	**2h(2)**		
	Frequency polarity	f_inv	BIN	**0**		
PSK	Symbol rate	JFS	[MHz]	**28.860**		
	Serial TS clock	f_{PSK}	[MHz]	65.536	**65.600**	66.400
	Clock frequency pull-in range	$\Delta f/f_{jCLK}$	[ppm]	**±200**		
	Carrier frequency pull-in range	f_{jAFC}	[MHz]	**±5**		
	Clock frequency Offset correction	jhkfrq	HEX(DEC)	6B55h (27,477)	**6BB0h (27,568)**	701Fh (28,703)
	Carrier AFC loop gain correction	afcg	HEX(DEC)	4Ch (76)	**4Ch (76)**	4Bh (75)

10.3 4MHz IF Mode (XT=4MHz)

XSEL1=1, XSEL0=0				Standard Clock (Crystal) Frequency [MHz]
Item		Symbol	Unit	**4.000**
Master clock frequency		MD	[MHz]	**78.000**
OFDM	IF frequency	IF	[MHz]	**4.063**
	Data frequency	FS	[MHz]	**65.015873**
	Serial TS clock	f_{OFDM}	[MHz]	**39.000**
	Clock frequency pull-in range	$\Delta f/f$	[ppm]	**±203**
	Carrier frequency pull-in range	f_{AFC}	[kHz]	**±250**
	Standard clock division ratio	iexdiv	HEX(DEC)	**02h (2)**
	PLL division ratio	ilpdiv	HEX(DEC)	**27h (39)**
	Clock frequency Offset correction	hkfrq	HEX(DEC)	**3320h (13,088)**
	Carrier frequency Offset correction	cpld_dt	HEX(DEC)	**0D56h(3,414)**
	Carrier AFC loop gain correction	affrq	HEX(DEC)	**0AAh(170)**
	Digital filter	lpfsl	HEX(DEC)	**0h(0)**
	Frequency polarity	f_inv	BIN	**0**
PSK	Symbol rate	JFS	[MHz]	**28.860**
	Serial TS clock	f_{PSK}	[MHz]	**62.400**
	Clock frequency pull-in range	$\Delta f/f_{jCLK}$	[ppm]	**±200**
	Carrier frequency pull-in range	f_{jAFC}	[MHz]	**±5**
	Clock frequency Offset correction	jhkfrq	HEX(DEC)	**59F2h (23,026)**
	Carrier AFC loop gain correction	afcg	HEX(DEC)	**50h (80)**

10.4 4MHz IF Mode (XT=27MHz)

XSEL1=0, XSEL0=0				Standard Clock (Crystal) Frequency [MHz]
Item		Symbol	Unit	27.000
Master clock frequency		MD	[MHz]	81.000
OFDM	IF frequency	IF	[MHz]	4.063
	Data frequency	FS	[MHz]	**65.015873**
	Serial TS clock	f_{OFDM}	[MHz]	40.500
	Clock frequency pull-in range	$\Delta f/f$	[ppm]	±196
	Carrier frequency pull-in range	f_{AFC}	[kHz]	**±250**
	Standard clock division ratio	iexdiv	HEX(DEC)	**0Bh (11)**
	PLL division ratio	ilpdiv	HEX(DEC)	**21h (33)**
	Clock frequency Offset correction	hkfrq	HEX(DEC)	3EF0h (16,112)
	Carrier frequency Offset correction	cpld_dt	HEX(DEC)	0CD8h (3,288)
	Carrier AFC loop gain correction	affrq	HEX(DEC)	0CAh (202)
	Digital filter	lpfsl	HEX(DEC)	0h(0)
	Frequency polarity	f_inv	BIN	0
PSK	Symbol rate	JFS	[MHz]	**28.860**
	Serial TS clock	f_{PSK}	[MHz]	64.800
	Clock frequency pull-in range	$\Delta f/f_{jCLK}$	[ppm]	**±200**
	Carrier frequency pull-in range	f_{jAFC}	[MHz]	**±5**
	Clock frequency Offset correction	jhkfrq	HEX(DEC)	6740h (26,432)
	Carrier AFC loop gain correction	afcg	HEX(DEC)	4Dh (77)

10.5 IQ Baseband Mode(XT=4MHz)

XSEL1=1, XSEL0=1				Standard Clock (Crystal) Frequency [MHz]
Item		Symbol	Unit	4.000
Master clock frequency		MD	[MHz]	78.000
OFDM	IF frequency	IF	[MHz]	0.000
	Data frequency	FS	[MHz]	65.015873
	Serial TS clock	f_{OFDM}	[MHz]	39.000
	Clock frequency pull-in range	$\Delta f/f$	[ppm]	±203
	Carrier frequency pull-in range	f_{AFC}	[kHz]	±250
	Standard clock division ratio	iexdiv	HEX(DEC)	02h (2)
	PLL division ratio	ilpdiv	HEX(DEC)	27h (39)
	Clock frequency Offset correction	hkfrq	HEX(DEC)	3320h (13,088)
	Carrier frequency Offset correction	cpld_dt	HEX(DEC)	0h(0)
	Carrier AFC loop gain correction	affrq	HEX(DEC)	0AAh(170)
	Digital filter	lpfsl	HEX(DEC)	0h(0)
	Frequency polarity	f_inv	BIN	0
PSK	Symbol rate	JFS	[MHz]	28.860
	Serial TS clock	f_{PSK}	[MHz]	62.400
	Clock frequency pull-in range	$\Delta f/f_{jCLK}$	[ppm]	±200
	Carrier frequency pull-in range	f_{jAFC}	[MHz]	±5
	Clock frequency Offset correction	jhkfrq	HEX(DEC)	59F2h (23,026)
	Carrier AFC loop gain correction	afcg	HEX(DEC)	50h (80)

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

The condition that AD_AVSS=AD_DVSS=JAD_AVSS=JAD_DVSS=JAD_LVSS=XOVSS=PLLVSS=VSS=0V should be observed as the standard.

Item	Symbol(Note 1)	Rating(Note 4)	Unit
Power supply voltage	VDDS	-0.3 - +3.9	V
	DR2VDD	-0.3 - +3.0	
	AD_DVDD	-0.3 - +3.0	
	JAD_DVDD	-0.3 - +3.0	
	AD_AVDD	-0.3 - +3.0	
	JAD_AVDD	-0.3 - +3.0	
	XOVDD	-0.3 - +3.0	
	PLLVDD	-0.3 - +3.0	
	VDDC	-0.3 - +1.7	
	DR1VDD	-0.3 - +1.7	
	JAD_LVDD	-0.3 - +1.7	
Input voltage	VINA	-0.3 - VDDS+0.3	V
	VINB	-0.3 - +5.5(Note 2)	
	AIN	0.0 - AD_AVDD	
	JAIN	0.0 - JAD_AVDD	
	XIN	0.0 - XOVDD	
Output voltage	VOUTA	-0.3 - VDDS+0.3	V
Input current	IIN	±10(Note 3)	mA
Storage temperature	Tstg	-40 - +125	°C

Note 1) VDDS, VINA, VOUTA: 3.3V interface rated value
VINB: 5V-tolerant interface rated value
DR1VDD, DR2VDD: DRAM cell rated value
AD_AVDD, AD_DVDD, JAD_AVDD, JAD_DVDD,
JAD_LVDD, X_VDD, PLL_VDD: Analog cell rated values
VDDC: Internal cell rated value
AIN: ADC input rated value for OFDM
JAIN: ADC input rated value for PSK
XIN: XI input rated value

Note 2) I^2C and SYRSTN pins are 5V input tolerable.

Note 3) Pins with pull-down and pull-up are excluded.

Note 4) This IC may malfunction if left for long periods under high electrical field conditions. Be sure to sufficiently separate the IC location from the CRT (by 20cm or more). If a sufficient distance cannot be maintained, shield the machine with a shield plate.

*** This product is of a low electrostatic withstanding strength. Use special care for handling.**

11.2 Operating Conditions

The condition that AD_AVSS=AD_DVSS=JAD_AVSS=JAD_DVSS=JAD_LVSS=XOVSS=PLLVSS=VSS=0V should be observed as the standard.

Item	Symbol	Minimum	Typ.	Maximum	Unit
Power supply voltage	VDDS	3.0	3.3	3.6	V
	DR2VDD	2.3	2.5	2.7	
	AD_DVDD	2.3	2.5	2.7	
	JAD_DVDD	2.3	2.5	2.7	
	AD_AVDD	2.3	2.5	2.7	
	JAD_AVDD	2.3	2.5	2.7	
	XOVDD	2.3	2.5	2.7	
	PLLVDD	2.3	2.5	2.7	
	VDDC	1.1	1.2	1.35	
	DR1VDD	1.1	1.2	1.35	
	JAD_LVDD	1.1	1.2	1.35	
Master clock frequency(Note)	MD	76.157	–	83.000	MHz
Clock duty ratio	Duty	45	50	55	%
Clock input level	XIN	0.5	–	XOVDD	Vp-p
Operating ambient temperature	Ta	-20	–	+85	°C

Note) The operating frequency differs according to clock operation mode.

[Important] **Normal demodulation operation cannot be ensured if the master clock frequency falls below the lower limit value (76.157MHz).**
Make sure that the master clock MD is always above the lower limit value with consideration to the center frequency deviation and age deterioration of the crystal.

11.3 Electrical Characteristics (DC Characteristics)

The condition that AD_AVSS=AD_DVSS=JAD_AVSS=JAD_DVSS=JAD_LVSS=XOVSS=PLLVSS=VSS=0V should be observed as the standard.
Unless otherwise specified, VDDC=DR1VDD=JAD_LVDD=1.2V, AD_AVDD=AD_DVDD= JAD_AVDD=JAD_DVDD =DR2VDD=XOVDD=PLLVDD=2.5V, VDDS=3.3V, and Ta=25°C.

Symbol	Item		Condition	Minimum	Typ.	Maximum	Unit	Applicable Pin
VIH	High level input voltage	3.3V I/F	–	2.0	–	–	V	1),2),3),5)
		5V I/F	–	0.8VDDS	–	–		6)
VIL	Low level input voltage	3.3V I/F	–	–	–	0.8	V	1),2),3),5)
		5V I/F	–	–	–	0.2VDDS		6)
IIH	High level input current	3.3V I/F	VINA=VDDS	-10	–	10	µA	1),2)
				10	–	200		3),5)
		5V I/F	VINB=VDDS	-10	–	10		6)
IIL	Low level input current	3.3V I/F	VINA=VSS	-10	–	10	µA	1),3),5)
				-200	–	-10		2)
		5V I/F	VINB=VSS	-10	–	10		6)
IOZ	Output leak current	3.3V I/F	VOUTA=VDDS or VSS	-10	–	10	µA	4)
				10	–	200		5)
		5V I/F		-10	–	10		6)
VOH	High level output voltage	3.3V I/F	IOH=-4mA	VDDS-0.6	–	–	V	4),5)
			IOH=-1µA	VDDS-0.05	–	–		
		5V I/F	IOH=-4mA	VDDS-0.6	–	–		6)
			IOH=-1µA	VDDS-0.05	–	–		
VOL	Low level output voltage	3.3V I/F	IOL=4mA	–	–	0.4	V	4),5)
			IOL=1µA	–	–	VSS+0.05		
		5V I/F	IOL=4mA	–	–	0.4		6)
			IOL=1µA	–	–	VSS+0.05		
AD_VREFP	OFDM ADC reference voltage 1		When AD_VREF and AD_CM are connected	–	1.4 x AD_CM	–	mV	N12
AD_CM	OFDM ADC reference voltage 2		–	–	0.5 x AD_AVDD	–	mV	M10
AD_VREFN	OFDM ADC reference voltage 3		When AD_VREF and AD_CM are connected	–	0.6 x AD_CM	–	mV	M11
AIN	OFDM ADC input amplitude		Differential	–	0.5	–	Vp-p	7)
			Single-ended	–	1.0	–		
AIN_DC	OFDM ADC input DC voltage		–	–	1.25	–	V	7)
JAD_CM	PSK ADC reference voltage		–	–	0.5 x AD_AVDD	–	mV	R6
JAIN	PSK ADC input amplitude		Differential	–	0.375	–	Vp-p	8)
			Single-ended	–	0.75	–		
JAIN_DC	PSK ADC input DC voltage		–	–	1.25	–	V	8)
XIN	XI input amplitude		–	0.5	–	XOVDD	Vp-p	R9
XOUT	XO and XCKO output amplitude		–	1.0	–	XOVDD	Vp-p	R7,R8
FIL	FIL output DC voltage		–	PLLVSS	–	PLLVDD	V	R10
IDDC	DR1VDD, VDDC, JAD_ LVDD current consumption (Note 1)		1.35V (standard 1.2V)	–	120 (Note 2)	207	mA	–
IDDS	VDDS current consumption (Notes 1 and 3)		3.6V (standard 3.3V)	–	10 (Note 2)	12	mA	–
IDD2D	DR2VDD, AD_DVDD, JAD_DVDD current consumption (Note 1)		2.7V (standard 2.5V)	–	8 (Note 2)	10	mA	–
IDDA	J JAD_AVDD, PLLVDD, AD_AVDD, XOVDD current consumption (Note 1)		2.7V (standard 2.5V)	–	45 (Note 2)	50	mA	–

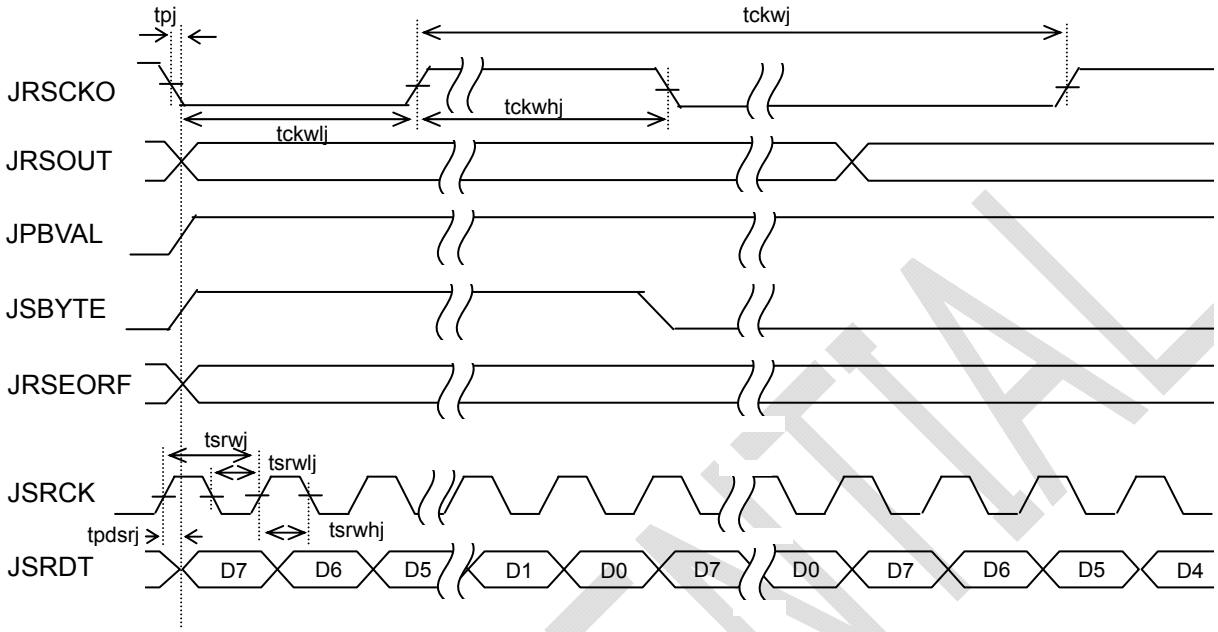
Applicable Pin

1) **B1, B2**
2) **A2, A3, D3**
3) **B3, B14, C3, C7, C9, C12, C13, H1, H2, J1, J2, J14, J15, K1, K2, K14, K15, L2, L14, L15, M15, R15**
4) **A1, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13,**
   D14, D15, E14, E15, F14, F15, G14, G15, H14, H15
5) **C1, C2, D1, D2, E1, E2, F1, F2, G1, G2, L1, N1, N14, P15**
6) **B15, C14, C15, M1, M2, M14, N15**
7) **R11, R12, R13, R14**
8) **R2, R3, R4, R5**

Note 1) Direct IF mode operation (clock frequency: 25.4MHz), OFDM/PSK concurrent operation
Note 2) Standard power supply voltage condition
Note 3) Serial TS output, RF_AGC and RF/IF_AGC output

11.4 Electrical Characteristics (AC Characteristics)

11.4.1 TS Output Interface for Digital Satellite Demodulation



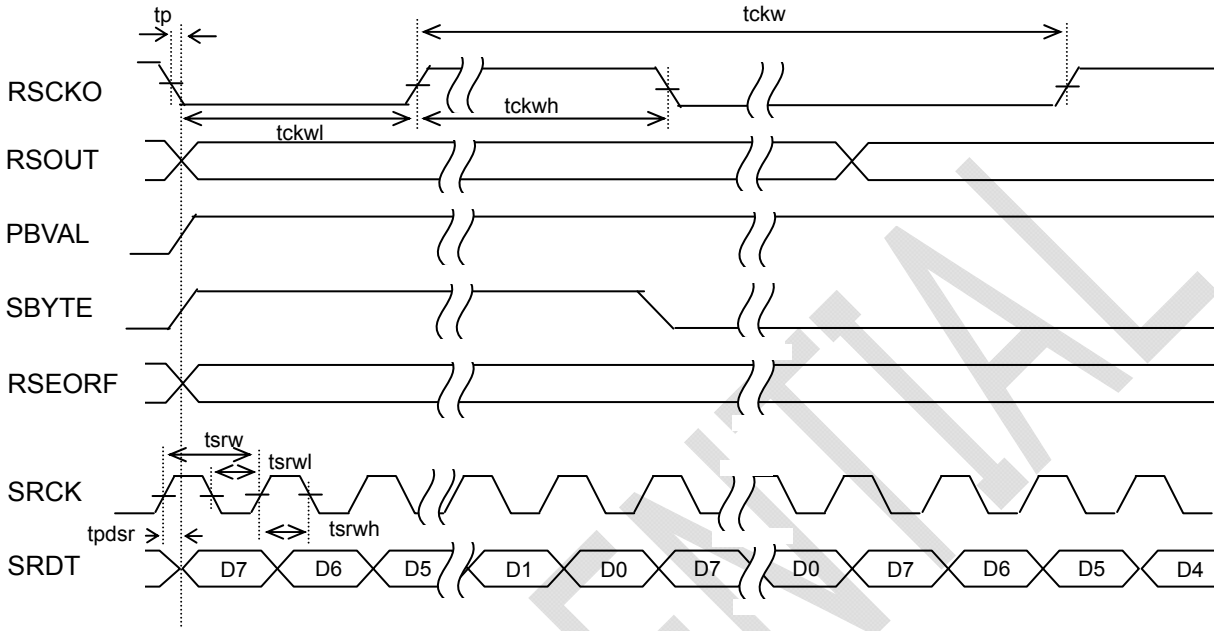
Item	Symbol	Condition	Standard Value			Unit
			Minimum	Typ.	Maximum	
Parallel TS clock cycle (Note 1)	tckwj	–	120	–	(Note 3)	ns
Parallel TS clock "H" cycle	tckwhj	–	56	–	–	ns
Parallel TS clock "L" cycle	tckwlj	–	56	–	–	ns
Data output delay time from parallel TS clock	tpj	from JRSCK0 rise JRSOUT[7:0],JPBVAL, JSBYTE, JRSEORF	-3	–	3	ns
Serial TS clock cycle (Note 2)	tsrwj	–	15	–	(Note 3)	ns
Serial TS clock "H" cycle	tsrwhj	–	6	–	–	ns
Serial TS clock "L" cycle	tsrwlj	–	6	–	–	ns
Data output delay time from serial TS clock	tpdsrj	From JSRCK rise JSRDT,JPBVAL, JSBYTE, JRSEORF	-3	–	2	ns

Note 1) JRSCKO is not a constant cycle. For the synchronization of data frequency and reference clock frequency, it is created from the thinned-out clock and the duty ratio changes.

Note 2) J JSRCK is not a constant cycle. For the synchronization of data frequency and reference clock frequency, it is created from the thinned-out clock and the duty ratio changes.

Note 3) Depends on the number of slots of the selected TS.

11.4.2 TS Output Interface for Digital Terrestrial Demodulation



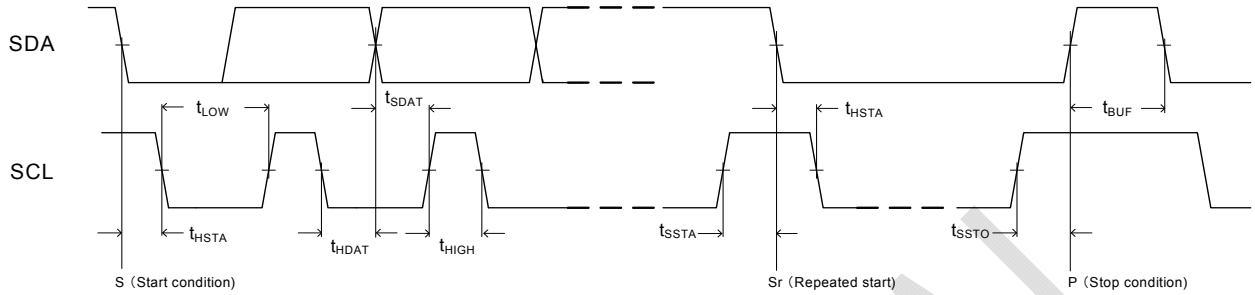
Item	Symbol	Condition	Standard Value			Unit
			Minimum	Typ.	Maximum	
Parallel TS clock cycle (Note 1)	tckw	–	196	–	296	ns
Parallel TS clock "H" cycle	tckwh	–	92	–	–	ns
Parallel TS clock "L" cycle	tckwl	–	92	–	–	ns
Data output delay time from serial TS clock	tp	From RSCK0 fall RSOUT[7:0],PBVAL, SBYTE, RSEORF	-3	–	3	ns
Serial TS clock cycle (Note 2)	tsrw	–	24	–	78.8	ns
Serial TS clock "H" cycle	tsrwh	–	10	–	–	ns
Serial TS clock "L" cycle	tsrwl	–	10	–	–	ns
Data output delay time from serial TS clock	tpdsr	From SRCK rise SRDT,PBVAL, SBYTE, RSEORF	-3	–	3	ns

Note 1) RSCKO is not a constant cycle. For the synchronization of data frequency and reference clock frequency, it is created from the thinned-out clock and the duty ratio changes.

Note 2) SRCK is not a constant cycle. For the synchronization of data frequency and reference clock frequency, it is created from the thinned-out clock and the duty ratio changes.

11.4.3 I2C Interface

The I^2C interface of TC90512 can operate on 400kHz. The same applies to through write and read for tuners.

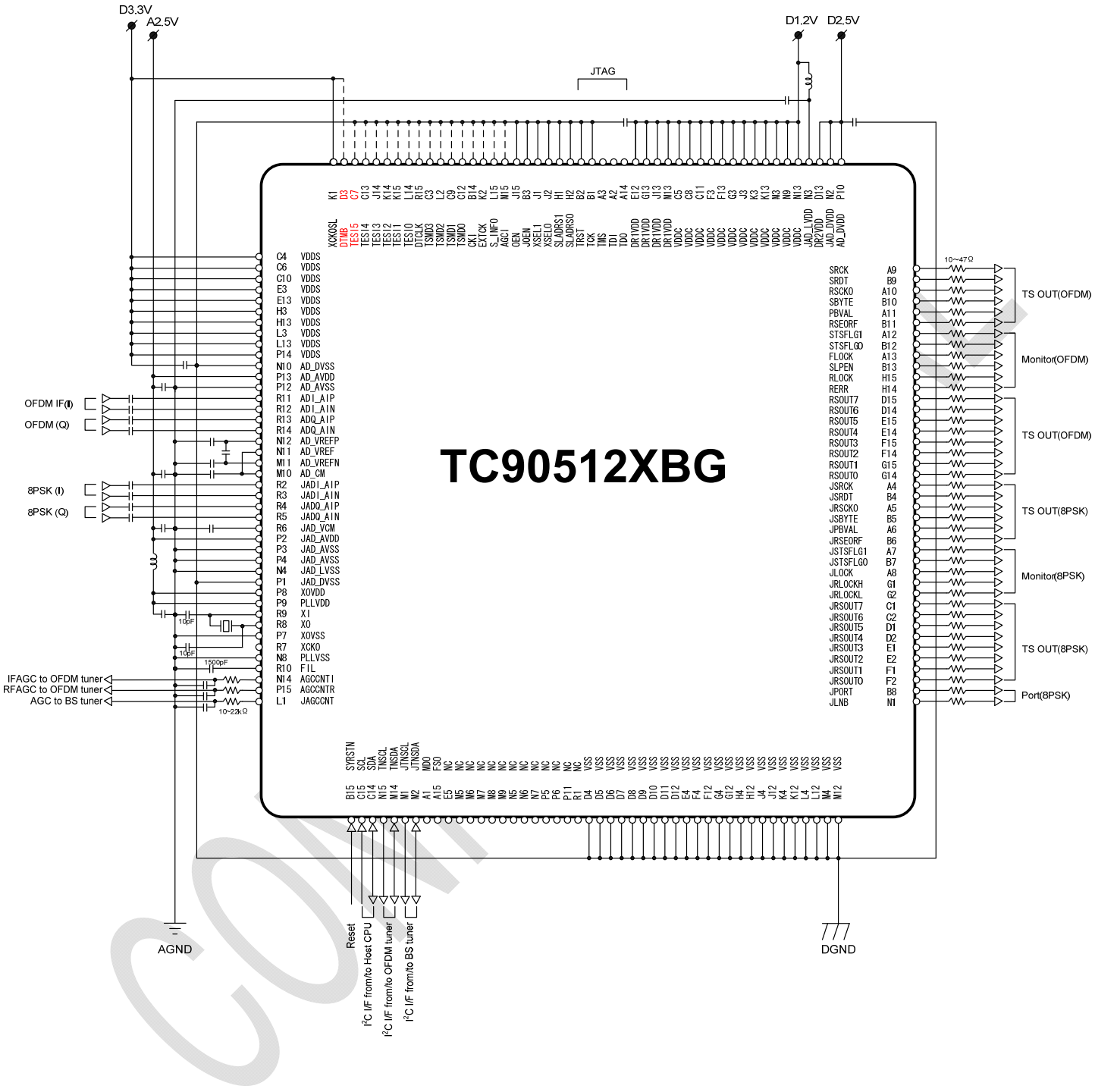


	Item	Symbol	Minimum	Typ.	Maximum	Unit
Bus	SCL clock frequency	f_{SCL}	0	–	400	kHz
	Start condition: hold time	t_{HSTA}	0.6	–	–	μs
	SCL clock “L” period	t_{LOW}	1.3	–	–	μs
	SCL clock “H” period	t_{HIGH}	0.6	–	–	μs
	Restart condition: setup time	t_{SSTA}	0.6	–	–	μs
	SDA data input: hold time	t_{HDAT}	0	–	–	μs
	SDA data input: setup time	t_{SDAT}	0.1	–	–	μs
	Stop condition: setup time	t_{SSTO}	0.6	–	–	μs
	Bus free time	t_{BUF}	1.3	–	–	μs

11.5 Power Supply Startup and Shutdown

Perform on/off operation of two or more power supplies simultaneously (within 100 ms). If this condition is not met, a malfunction or failure may be caused. (Note, however, that they need not be turned on or off in the order of their operating voltages.)

12. Application Circuit



* Constants shown in the figure are reference values.

* The analog GND should be separated from the digital GND. Each should be wholly grounded with a low impedance.

* The crystal and the oscillation capacitor should be placed close the XI and XO pins with shortest patterns.

* In the figure, the power supply bypass capacitor is indicated in a simplified form. The digital power supply should be bypassed to DGND and the analog power supply to AGND with a capacitor of approx. 0.1μF at a place closest possible to the pin.

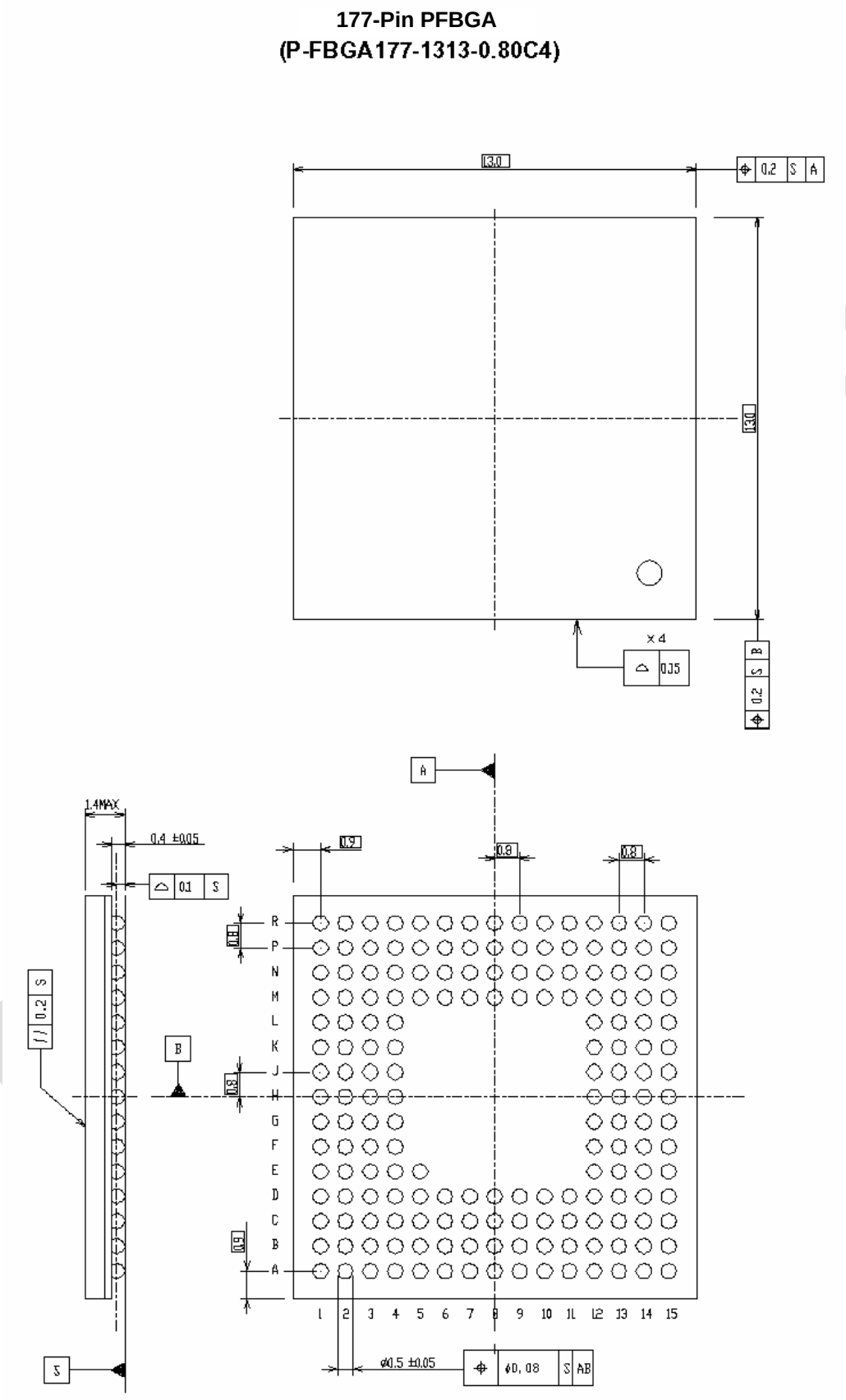
* The setting of XSEL1 and XSEL0 changes depending on the frequency of the crystal to be used.

* The TS output and monitor output can be turned ON or OFF separately. Outputs that are not needed should be turned OFF.

* Pins labeled NC are not connected to the chip. They can be connected to any pattern.
* Connections indicated by dashed lines can be omitted since the pertinent pins are pulled up or down.
* Using damping resistors in series with digital signal output may be effective in reducing spurious output. Use of a resistor of approx. 10kΩ to 20kΩ closest possible to the pin is effective for AGC control output.
* It is recommended to provide the analog 2.5V power supply and the digital 2.5V power supply (D2.5V) separately.
* It is recommended to provide PLLVDD and XOVDD after implementing isolation from the analog 2.5V power supply (A2.5V) by a coil, etc. for a measure against noises.
* It is recommended to provide JAD_LVDD after implementing isolation from the digital 1.2V power supply (D1.2V) by a coil, etc. for a measure against noises.

13. Package

177-Pin PFBGA
(P-FBGA177-1313-0.80C4)



Revision History

2006/06/15	rev.100		
2006/07/24	rev.101	8.3	Corrected the explanations of jtsld, jtslc, jtslb, and jtsla in the register list.
		8.4.2	Deleted (higher 32 bits) from the description of jhkfrq in the register list.
		9.4.2	Corrected the description of STSFLG1 and STSFLG0 in the Signal System Table.
2006/08/10	rev.102	11.4.3	Added an I2C timing chart (no changes are made from TC90502 in terms of usage).
2006/08/17	rev.103	Cover	Changed the power consumption typ from 350mW to 310mW.
		1.3	Changed the power consumption typ from 350mW to 310mW.
		2.	Corrected the description of recovery from standby.
		4.	Changed the description of pulling down SYRSTN, SCL, SDA, TNSCL, TNSDA, JTNSCL, and JTNSDA, changed the notes, and changed the remarks of XCKO.
		5.2.1	Added the addresses 51h, 52h, 53h, 5Ah, and 5Bh to the PSK demodulation register map.
		6.	Changed the description of adfs (changed the indication of differential voltages).
		6.1	3) Added the description of adfs to the ADC dynamic range. 4) Changed the specified input level to differential voltage 0.375Vp-p.
		6.4	Added XCKOSL to Figure 6.4, 6.5, and 6.6 and corrected the notes. Corrected the addresses of ixckosl and ixosl in the register list. Changed the XCKO output to a non-inverted clock.
		6.5	Added a description of OFDM IF frequencies. Corrected the description of iexdiv in the register list.
		6.7	Changed the description of JOEN (pulled in by isyrst).
		8.3	Corrected the description of jport in the register list and corrected the notes.
		8.3	Corrected the description of JRLOCKL and JRLOCKH. Added hselout to the register list.
		8.6	Added pllhmax (address 51h), pllbhgd (addresses 52h and 53h), and pllqhgd (addresses 5Ah and 5Bh) to the register list.
		8.6.1	Added descriptions of pllhmax, pllqhgd, and pllbhgd.
		9.3	Corrected the description of slplkmon in the register list (deleted the asterisks).
		9.7.1	Corrected the description of Item (3).
		9.9	Corrected the description of cpdmax, schnum, and initnum in the register list. Deleted sywsoff from the register list.
		9.9.4	Corrected the description of schnum and initnum.
		9.10	Corrected the description of gr1dly, gr2dly, and gr3dly in the register list.
		9.16	Changed the slot mode to the packet mode.
		9.16.8	Added the description of rulock and rmsk.
		9.17	Corrected the description of seqen in the register list.
		11.3	Changed the typ values of current consumption IDDA and IDD2D.
		11.4.1	Corrected the maximum value of the clock cycle and added notes.
		11.4.2	Corrected the maximum and minimum values of the clock cycle.
2006/08/22	rev.104	4.	Corrected the pin function J3 (VDDS to VDDC).
2006/09/13	rev.105	5.2.1	Changed the automatically set register initial values to XSEL in the register map. Added descriptions of automatic settings to the notes.
		5.2.2	Changed the automatically set register initial values to XSEL in the register map. Added descriptions of automatic settings to the notes. Changed the address 7Fh to "R" (READ) in the OFDM register map.
		6.4.3	Changed the description of ixosl in the register list.
		9.7.4	Corrected the initial value of lpsfl in the register list.
		9.7.5	Corrected the initial value of dpstep in the register list.
2006/10/05	rev.106	5.2.2	Changed the address C7h to "W" (WRITE) in the OFDM register map.

		11.3	Added the maximum value of current consumption.
		12.	Change the processing of TESI5 and DTMB in the application circuit diagram.
2006/10/20	rev.107	11.1	Corrected the maximum absolute rating and added a caution.
		p.2	Added a caution.
2006/10/20	rev.108	5.2.2	Changed the initial value of address 04h to XCKOSL in the OFDM register map, and changed the initial value of ixosl to 0 (not interlocked with XCKOSL).
2006/11/20	rev.109	5.2.2	Added the address 5Fh (plroff) to the OFDM register map.
		9.1.3	Added a description of PLR and a register list.
2006/11/23	rev.110	11.3	Changed the values of DC characteristics IIH (5V I/F) and IOZ (5V I/F). Changed the AD_CM typ. value to 0.5 x AD_AVDD.
2006/12/12	rev.111	8.1	Changed the description of psksyrst of the PSK demodulator. (Not only the power-on reset SYRSTN but also psksyrst= "1" are required.)
2007/01/16	rev.112	9.16.5	Changed the measurement cycle specified by the cyc register in time mode (Mode 3 only).
		9.16.6	Changed the measurement cycle specified by the cyc register in time mode (Mode 3 only).
2007/01/30	rev.113	4.	Corrected the remarks of AGCCNTR.
2007/02/28	rev.114	9.5.2	Changed the set values in 4MHz IF mode or IQ baseband mode (XT = 4MHz).
		11.4.1	Deleted JRSOUT from the conditions of tpdsrj and changed the maximum value to 2ns.
		9.16	Corrected the description of cyc in the register list.
		9.16.5	Corrected the setting range of the cyc register in Mode 1, Mode 2, and time mode.
		9.16.6	Corrected the setting range of the cyc register in Mode 1, Mode 2, and time mode.
2007/03/08	rev.115	8.3.4	Changed the description of emgcy operation when emgmsk="1" is set. (emgmsk="1" is not reflected on emgcy but on JSTSFLG0 only.)
2007/05/07	rev.116	P.2	Added notes.
2007/05/08	rev.117	5.2.1	Added tston to address 57h.
		8.10.2	Added a description of constellation output.